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Prior Art

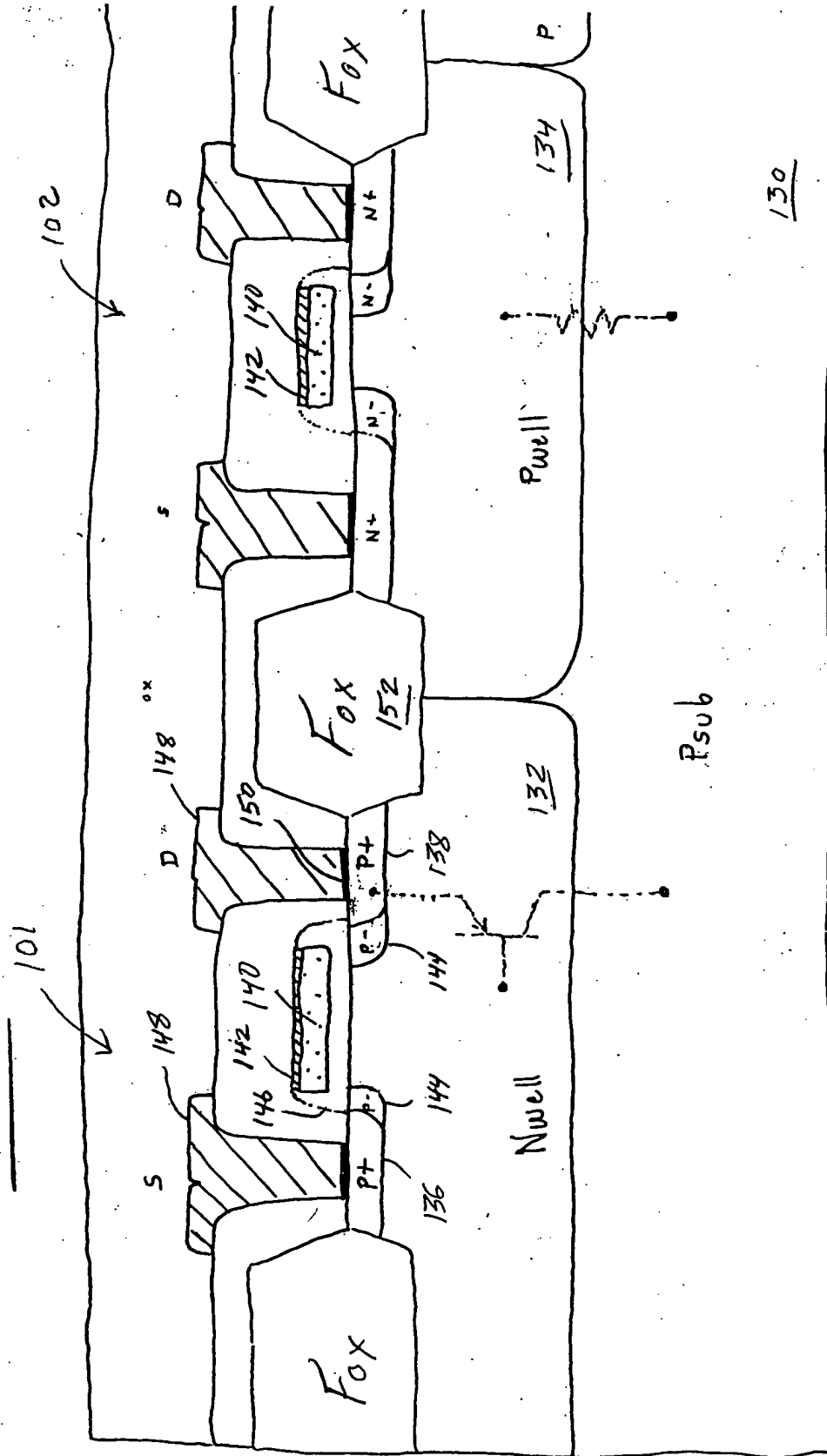


Fig. 1B

Prior Art

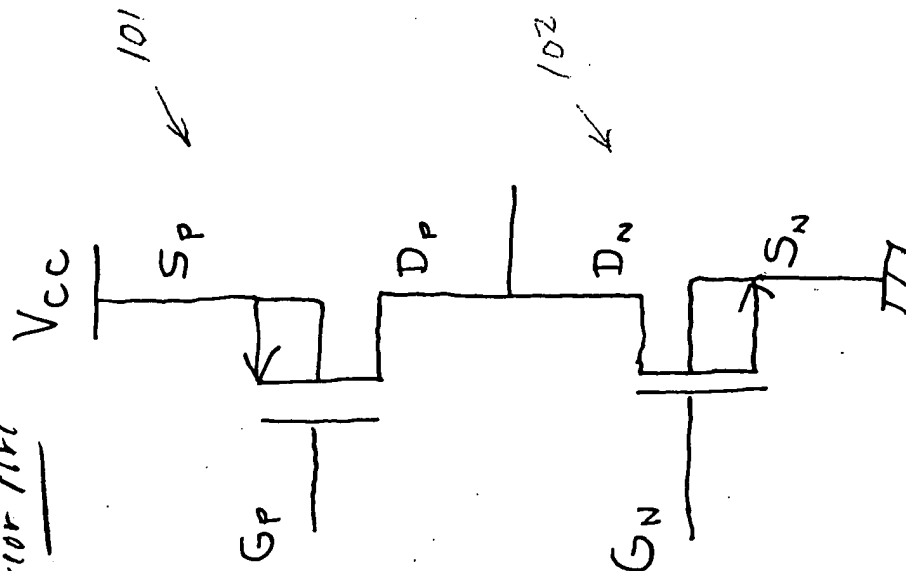
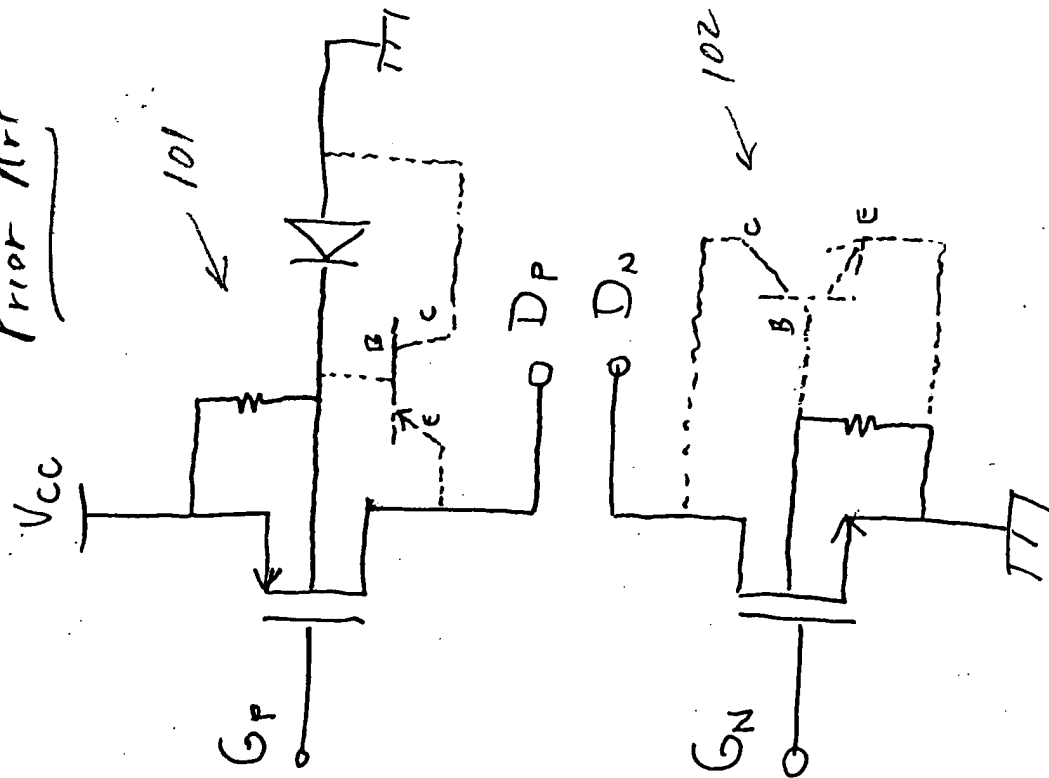


Fig. 1C

Prior Art



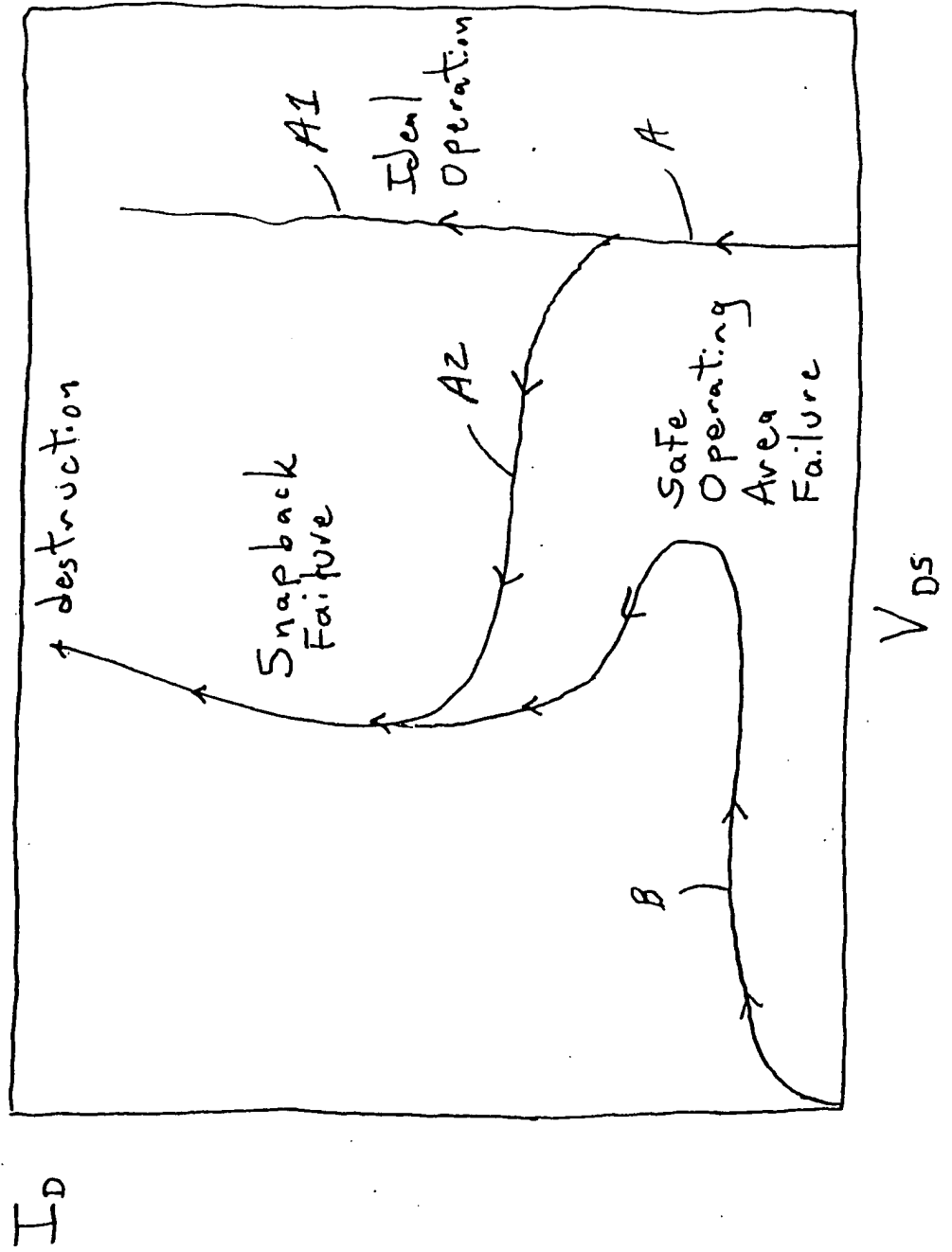




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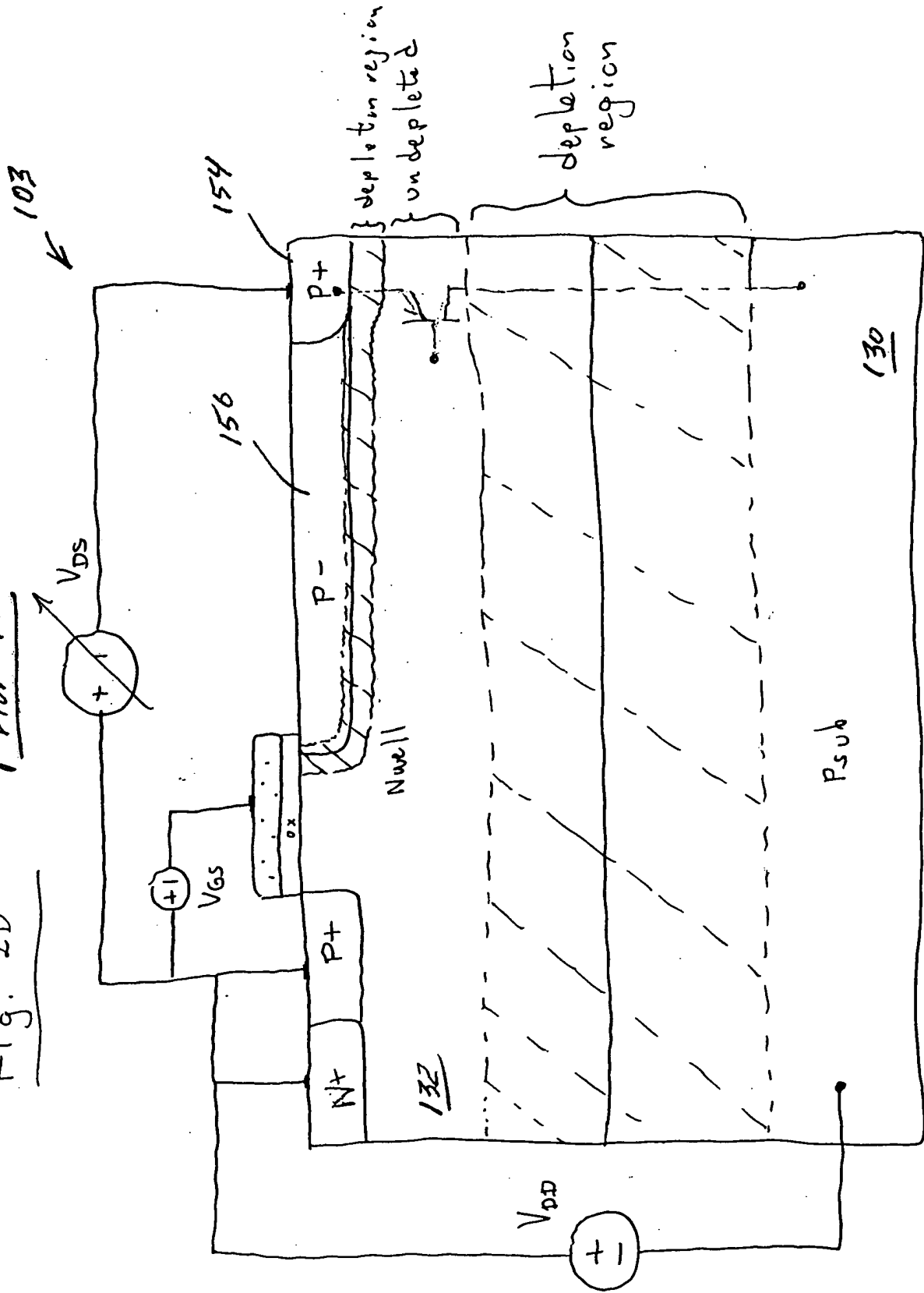
Fig 2C

Prior Art



Prior Art

Fig. 2D



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Fig. 3 Prior Art

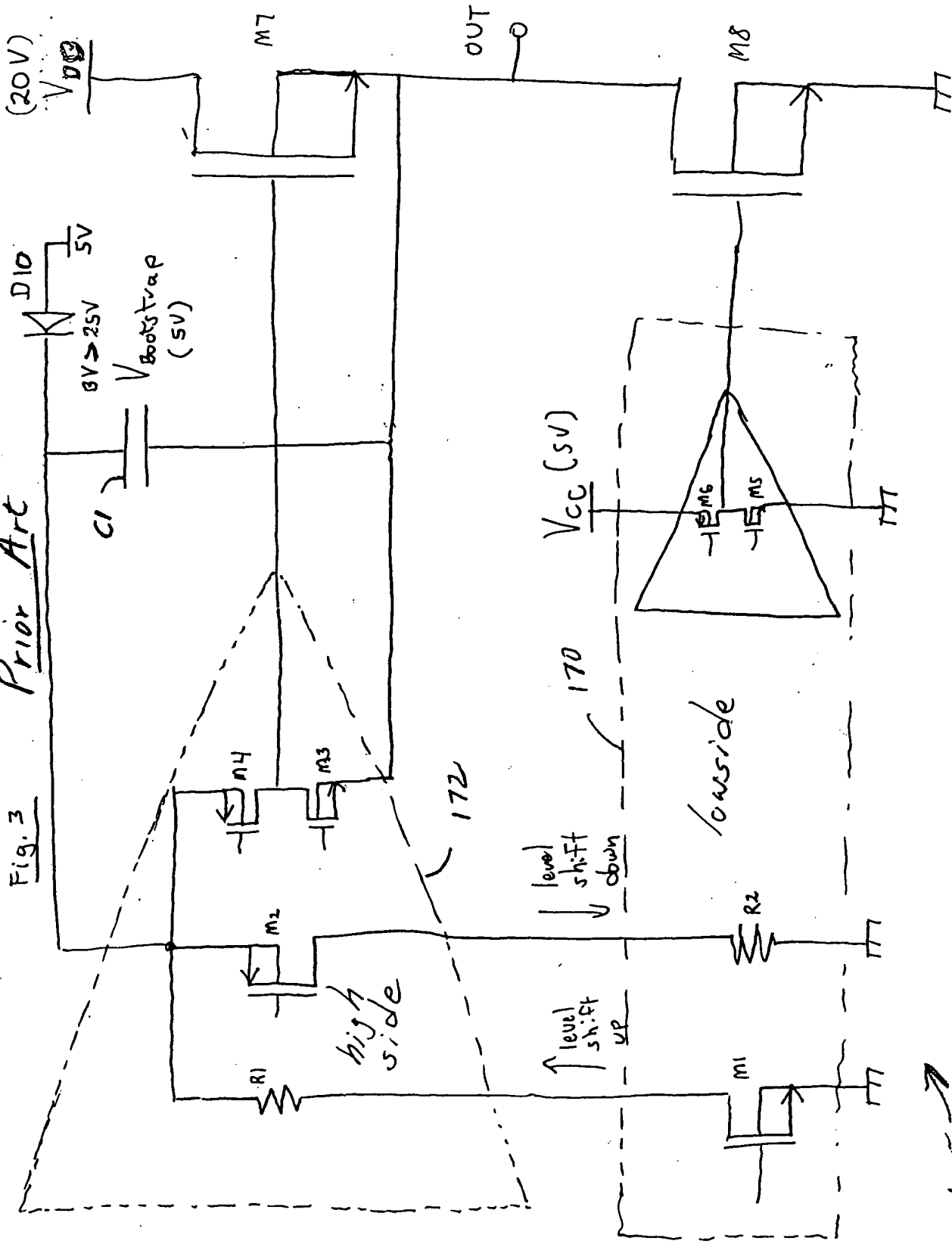




Fig. 4A

Prior Art

108

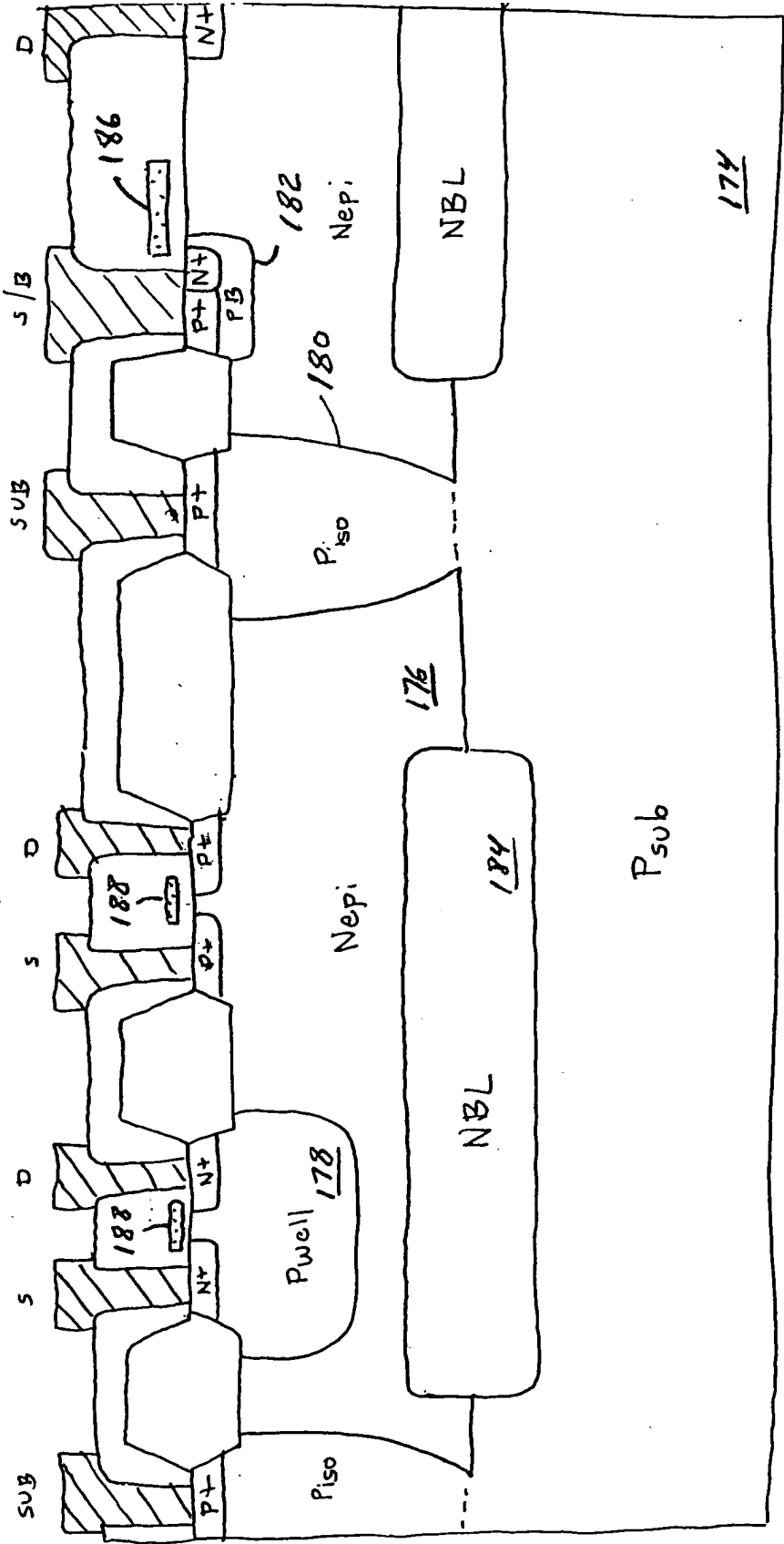
107

106

NMOS

PMOS

N-LDMOS



41B

109

Prior Art

N-ch QVDMOS

$$\frac{B}{S}$$

502B

Q

4/2/9

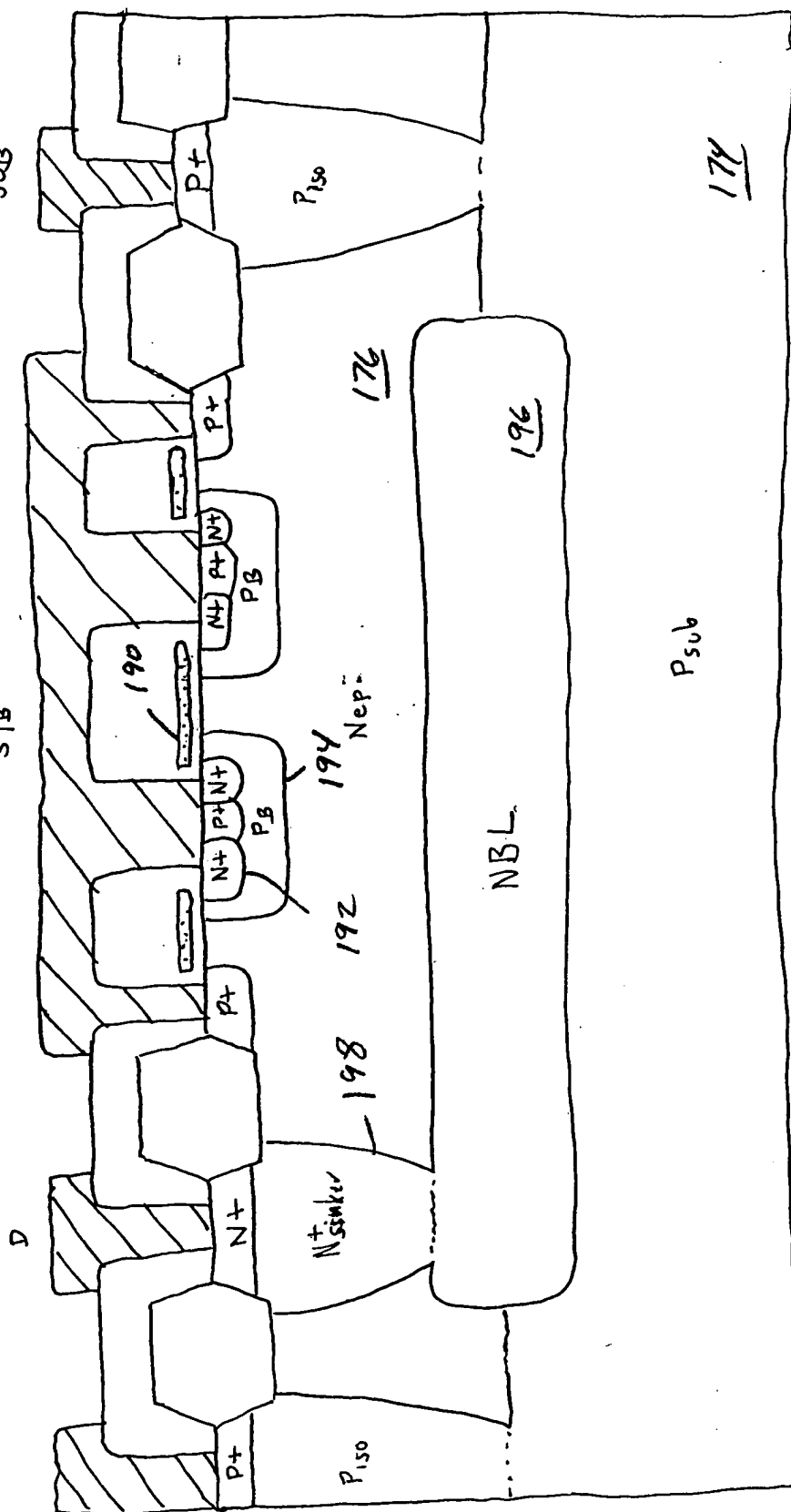




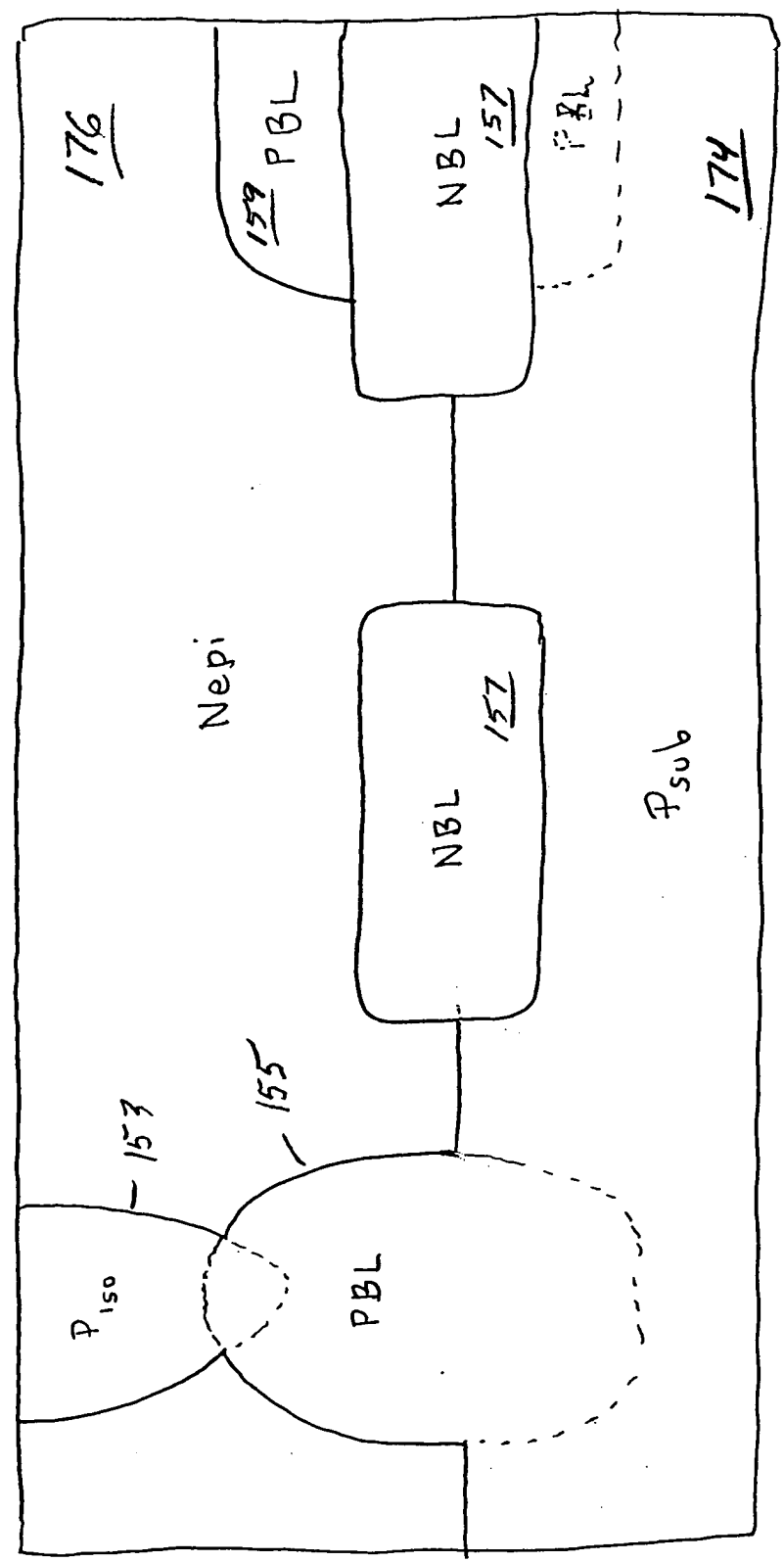
Fig. 5A

Prior Art

P<sub>4</sub> Buried Layer  
(isolated)

N<sub>4</sub> Buried Layer

isolation



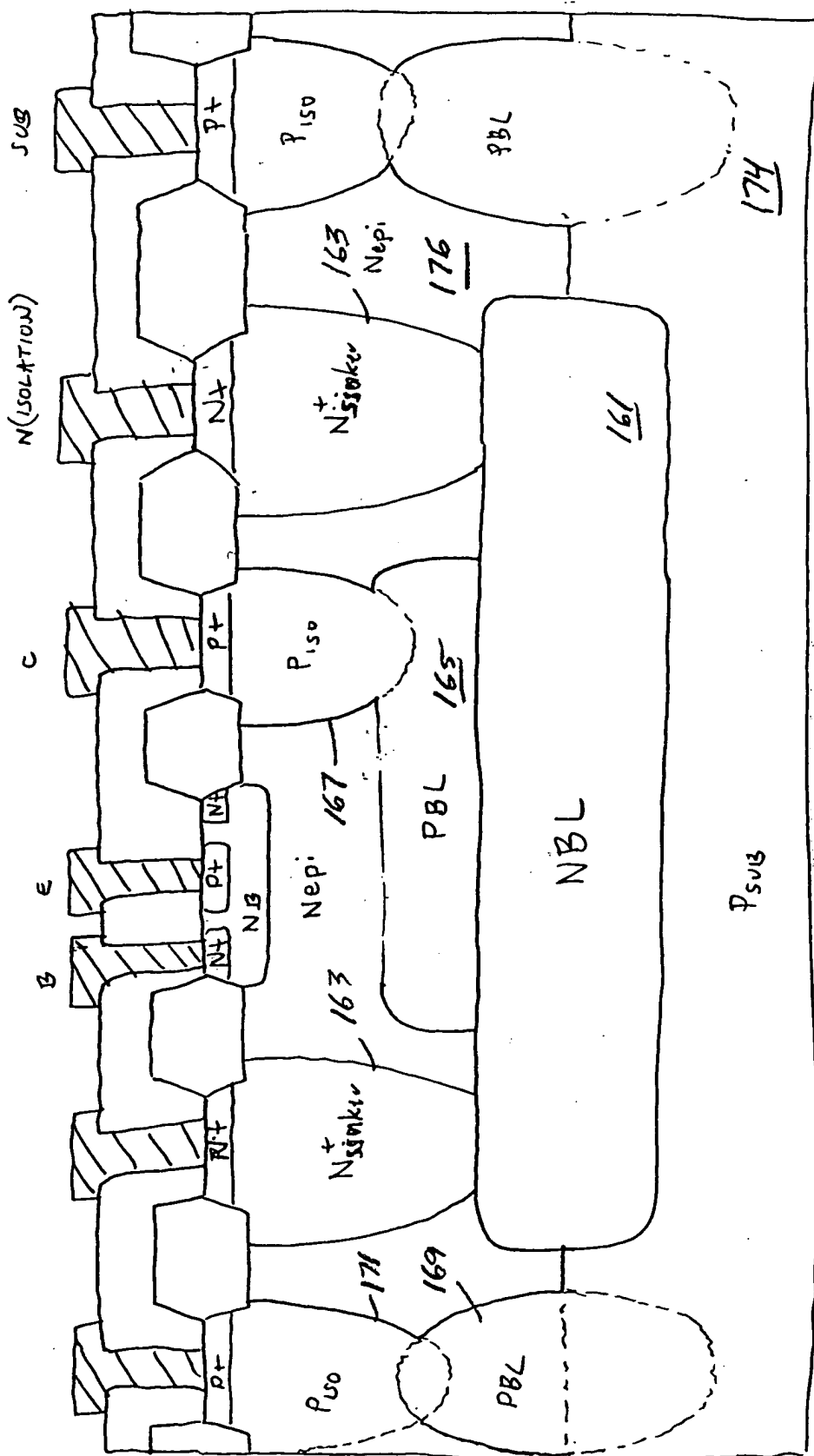
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Prior Art

Fig. 5B

112

PNP

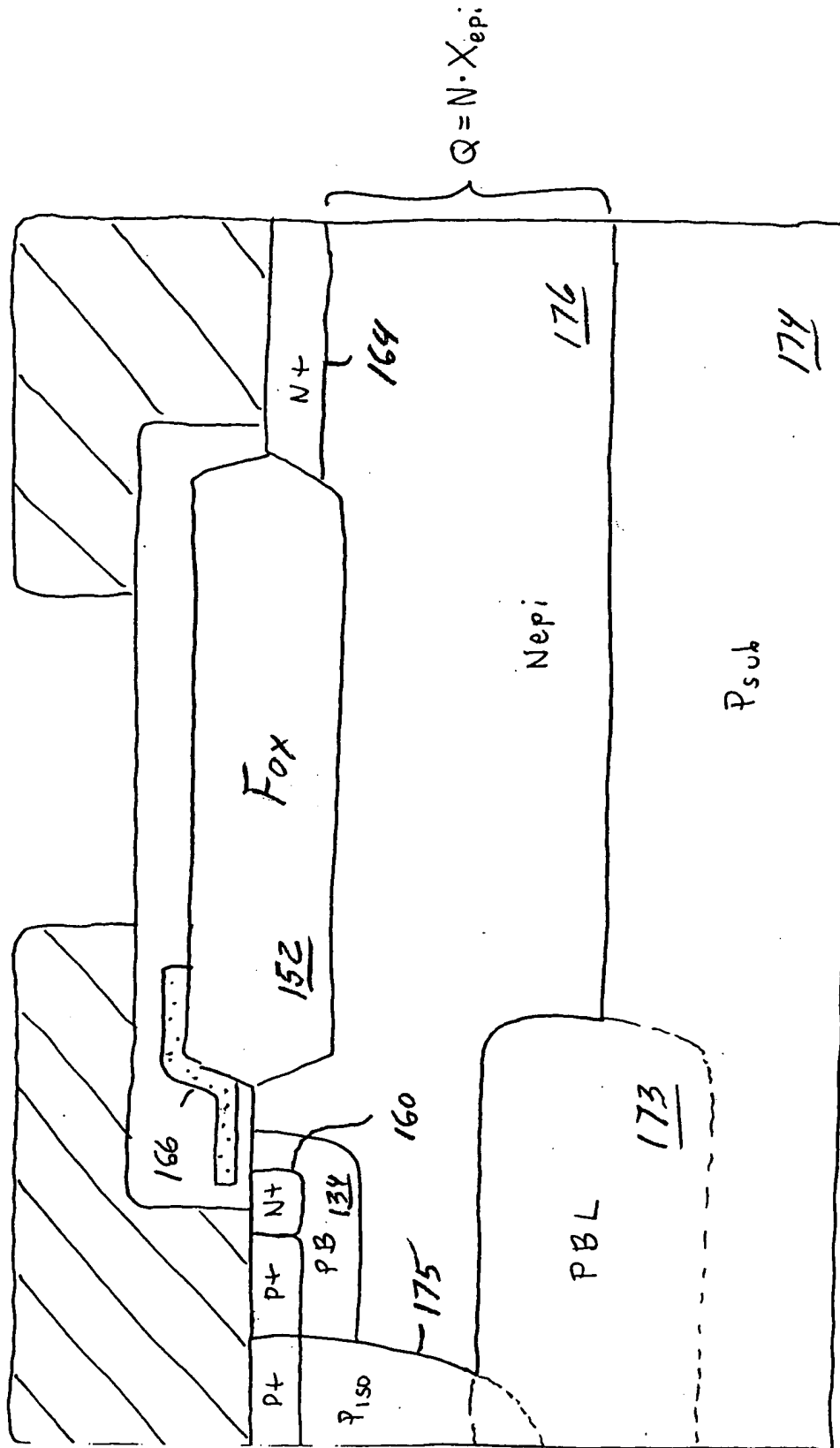


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Fig. 5C

Prior Art

104



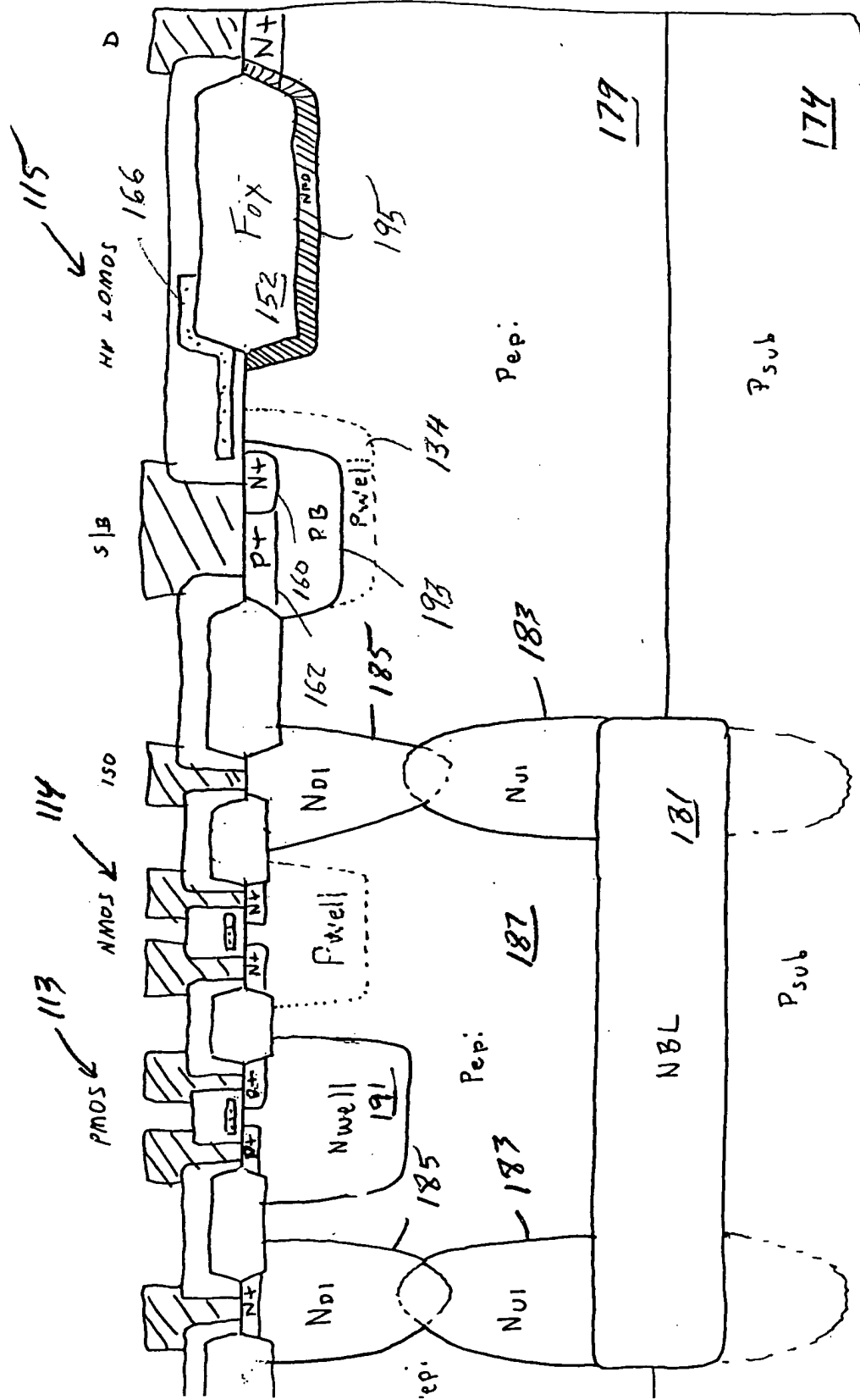
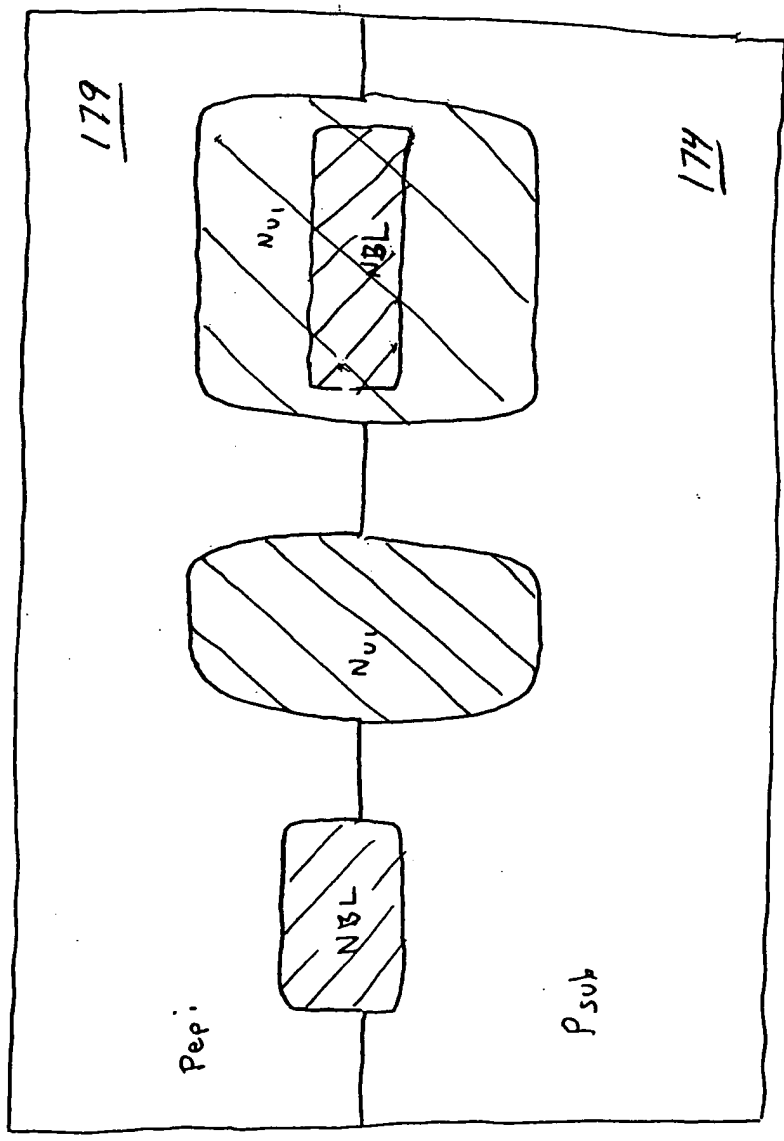






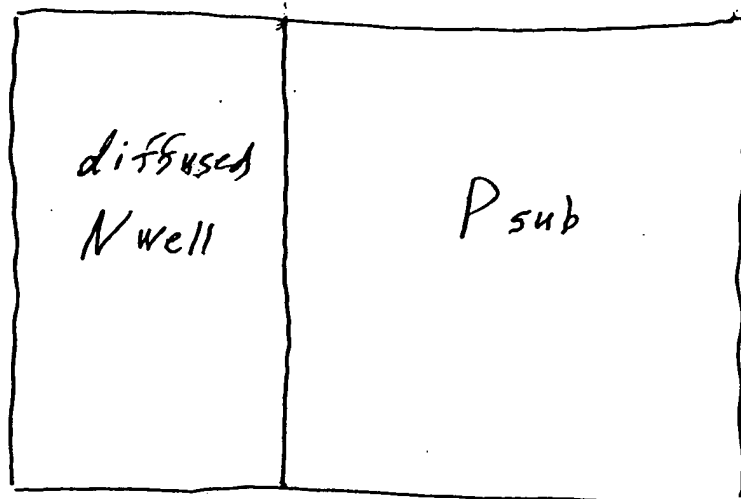
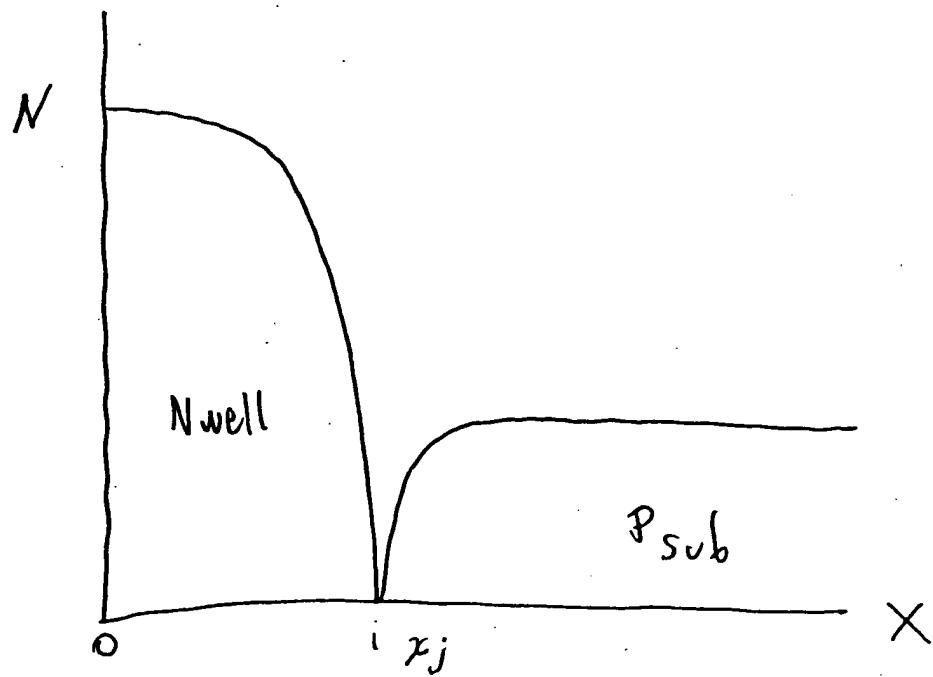
Fig. 6C

Prior Art



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Prior Art Fig. 7A



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Fig. 7B

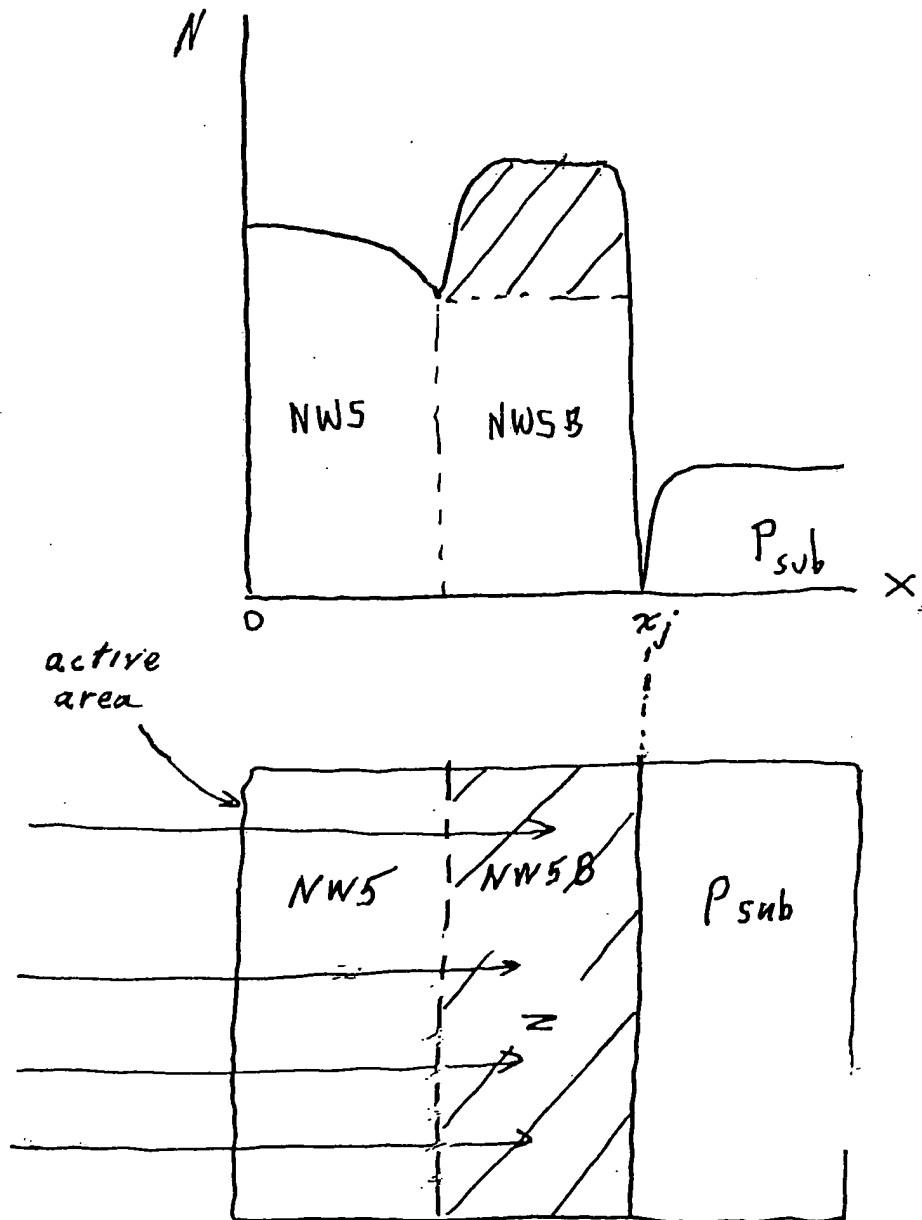
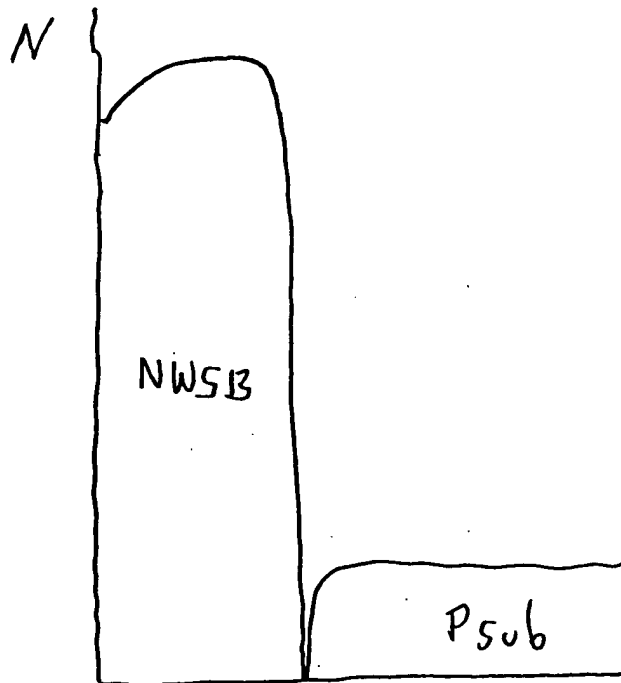


Fig. 7c

0

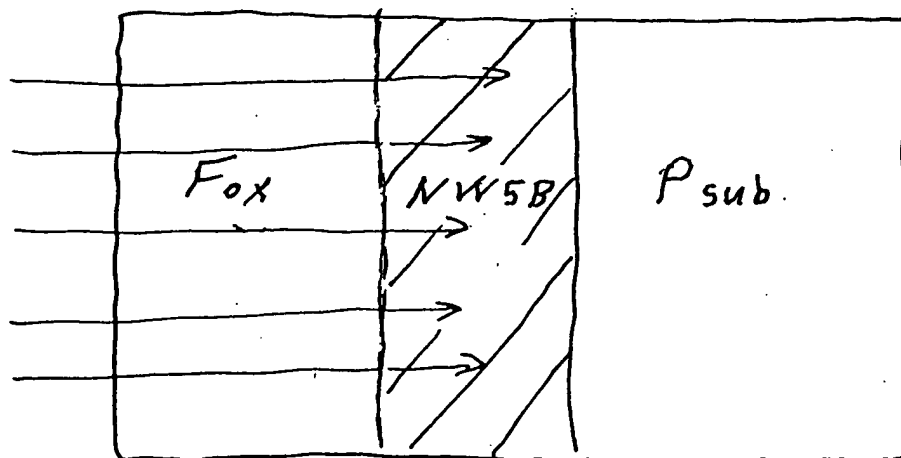


Fig. 8A

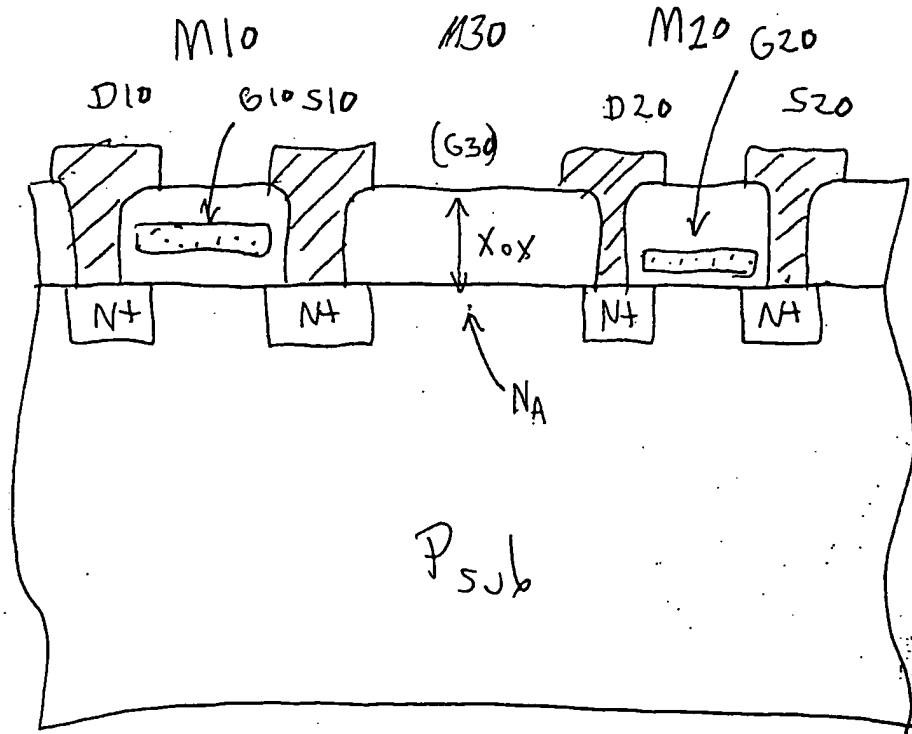
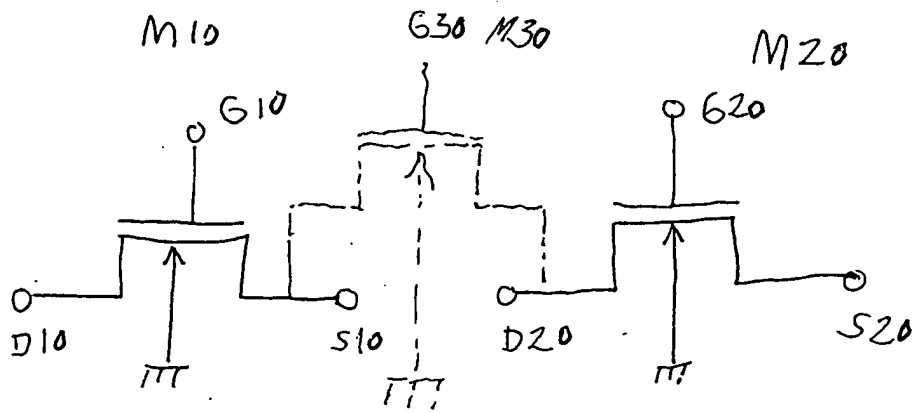


Fig. 8B



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Fig. 9B

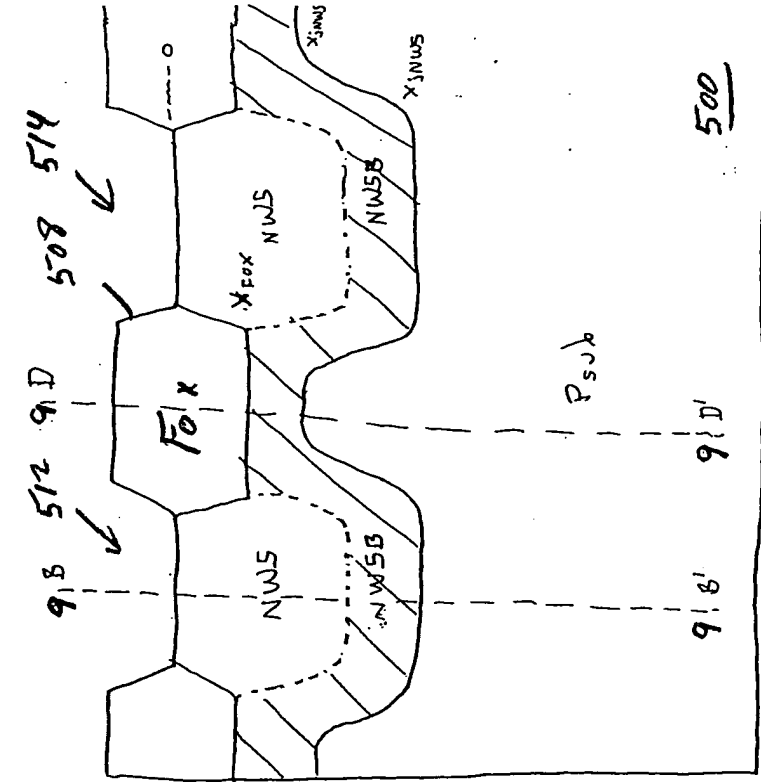
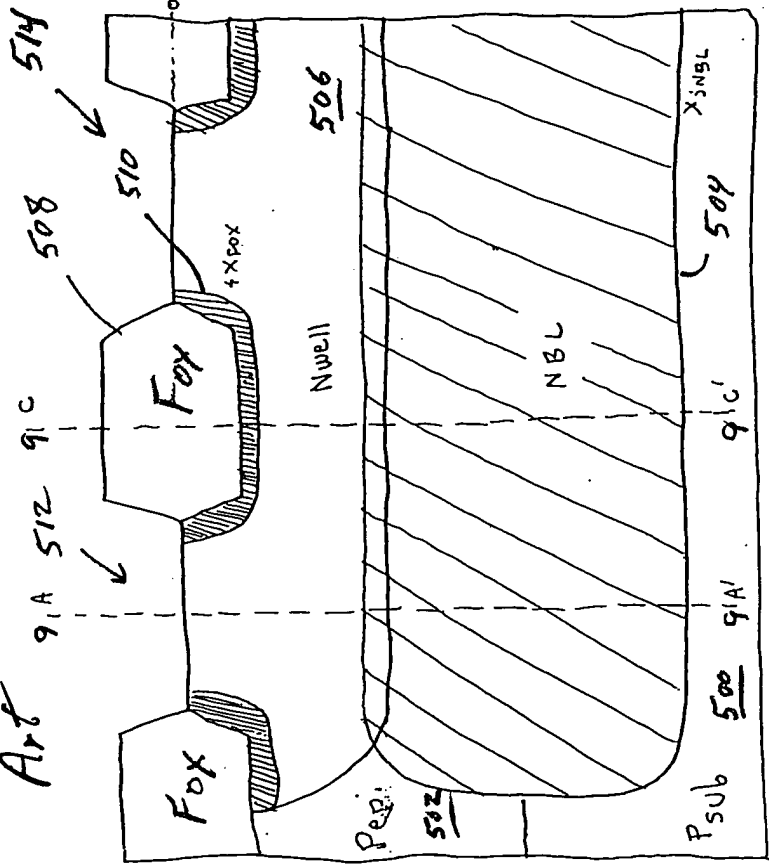


Fig. 9A

Prior Art



Prior Art

Fig. 9C

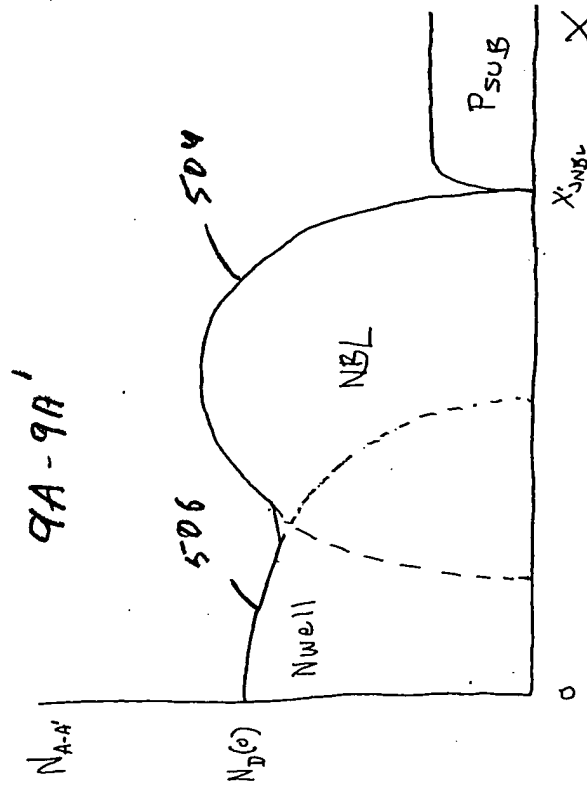
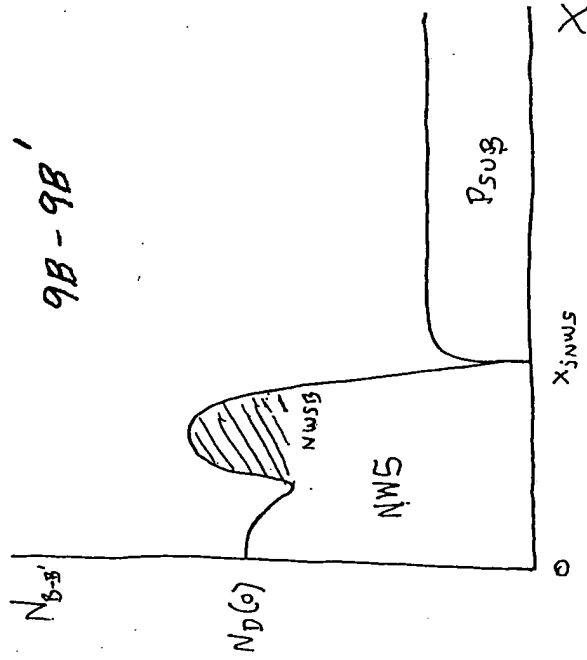
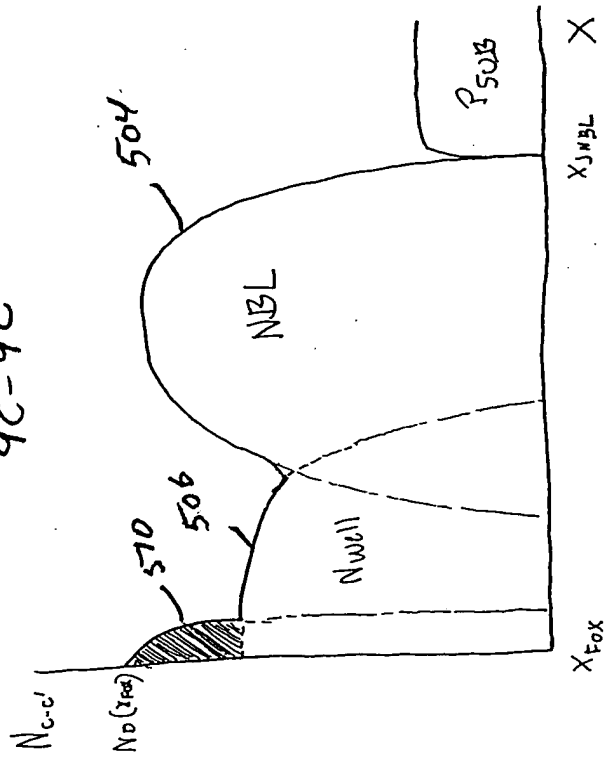


Fig. 9D



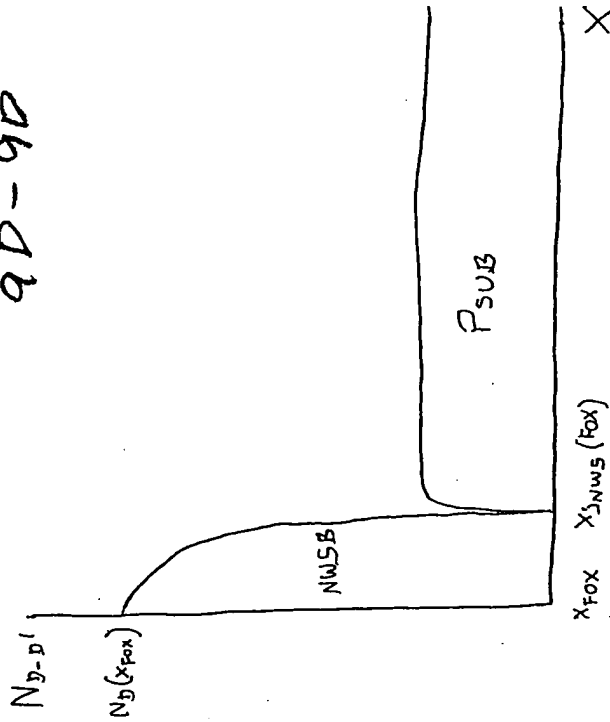
11-50

9C-9C'



11  
9  
-  
5  
11

9D-9D'





104

Prior Art

104

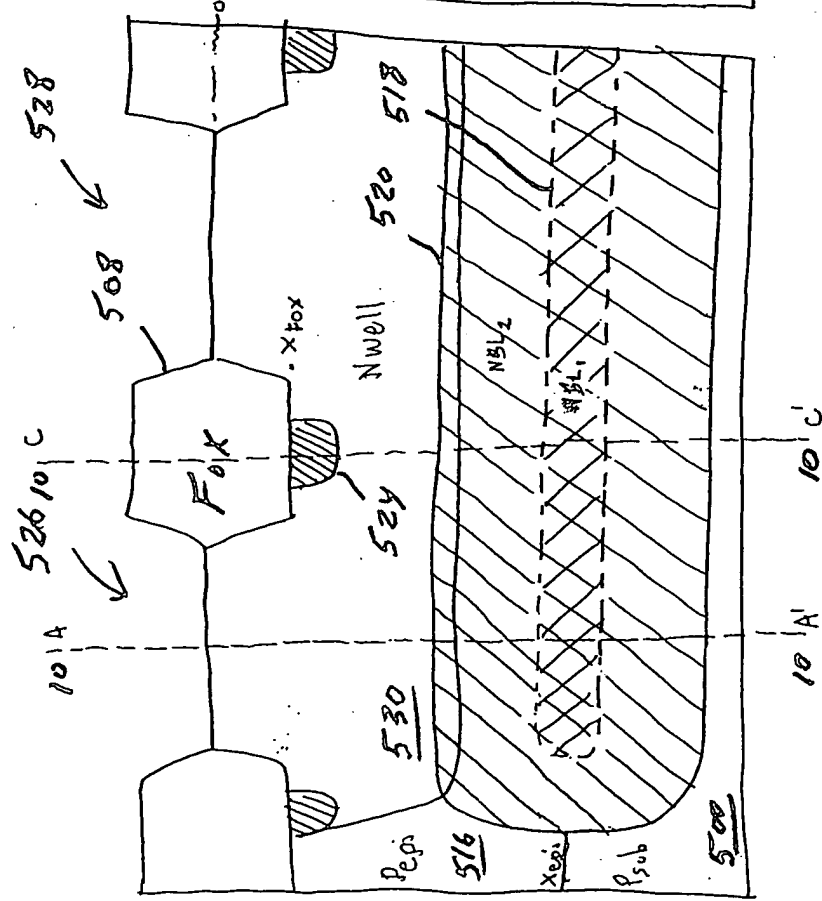
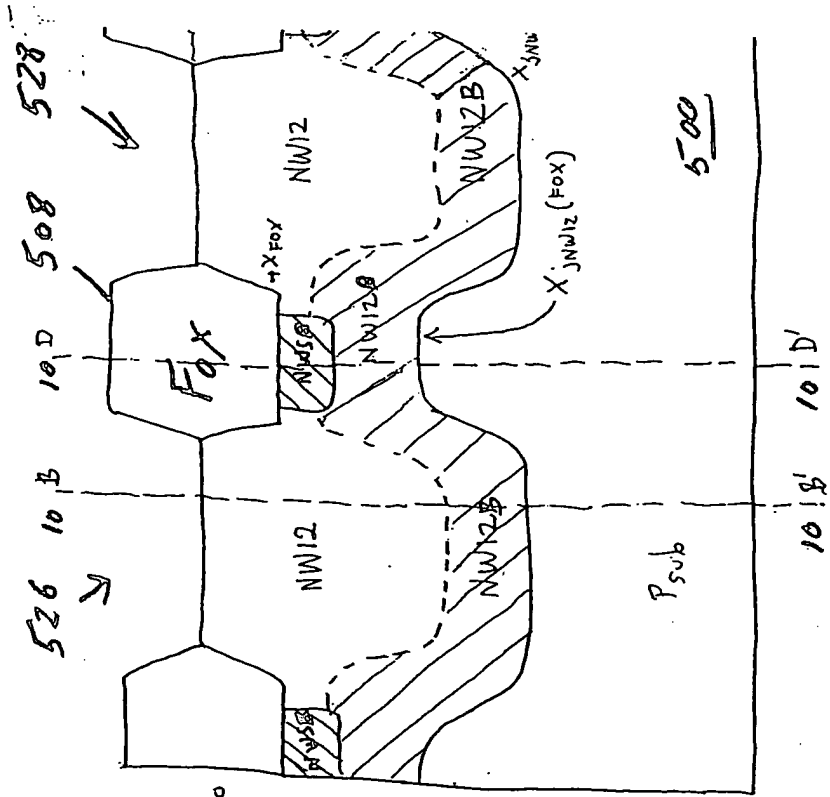


Fig. 10B



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Fig. 10D

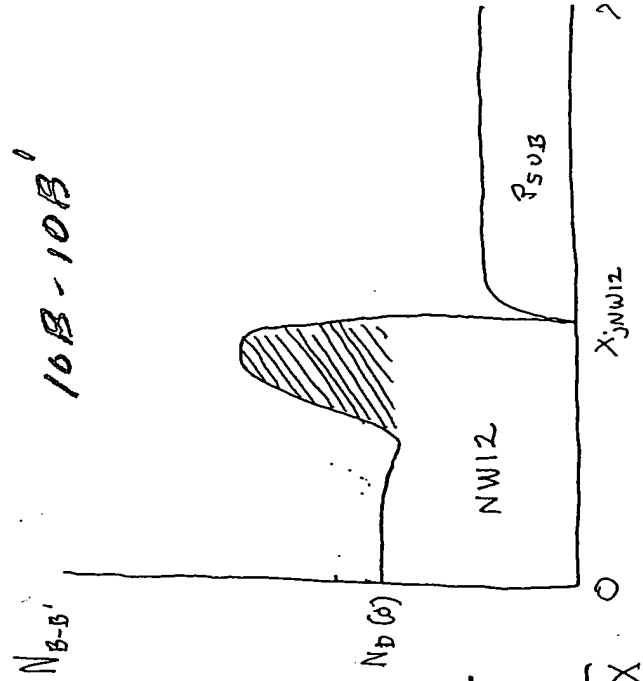


Fig. 10C

Prior

Art

10A-10A'

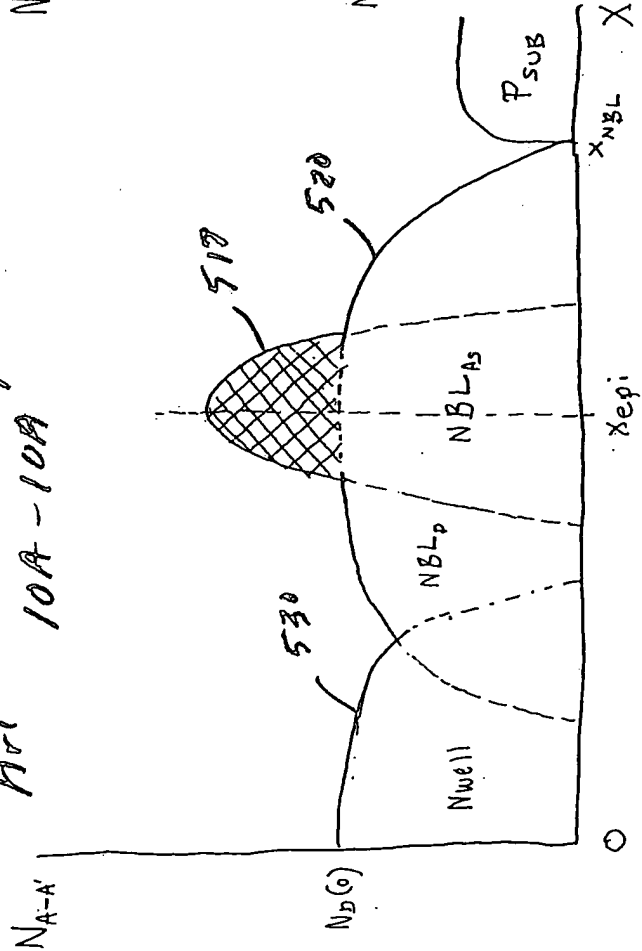


Fig. 10F

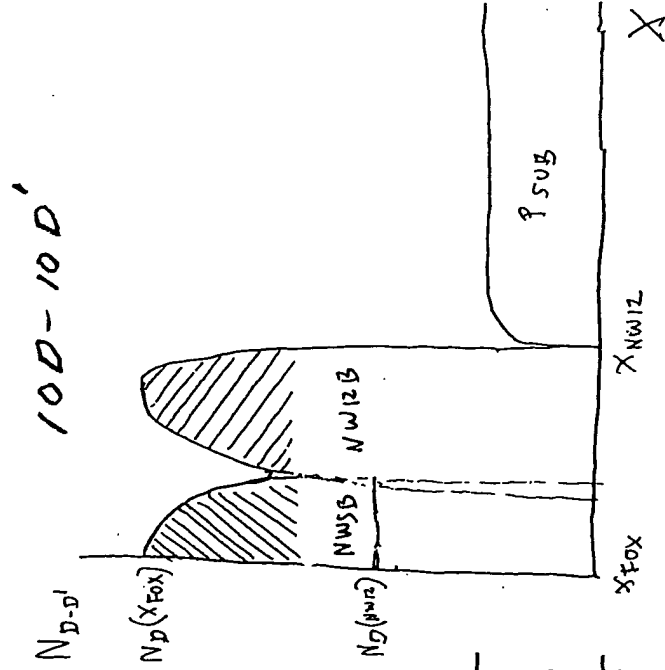


Fig. 10E

Prior Art

10C-10C'

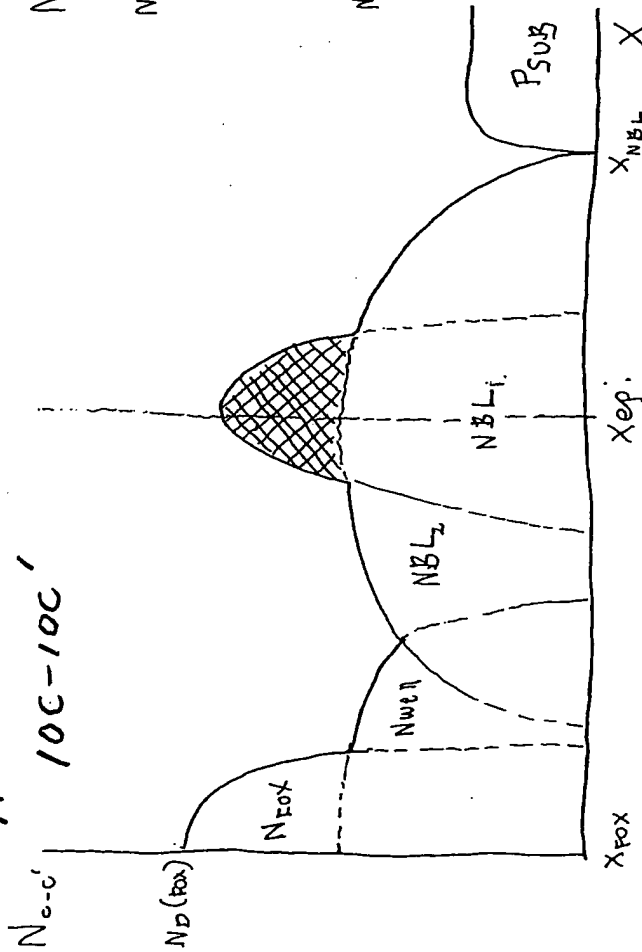


Fig. 10G

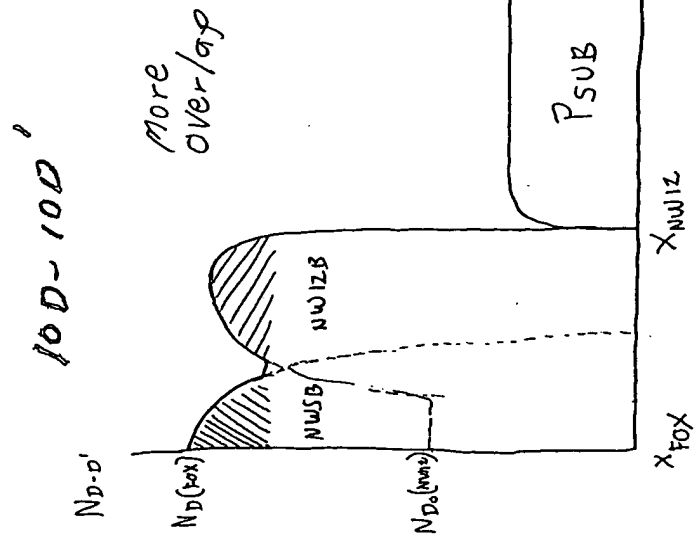


Fig. 10H

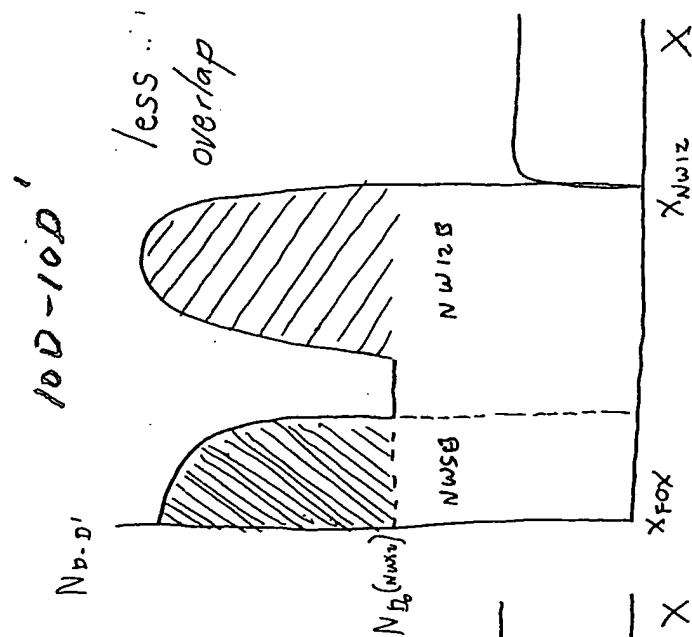


Fig. 10I

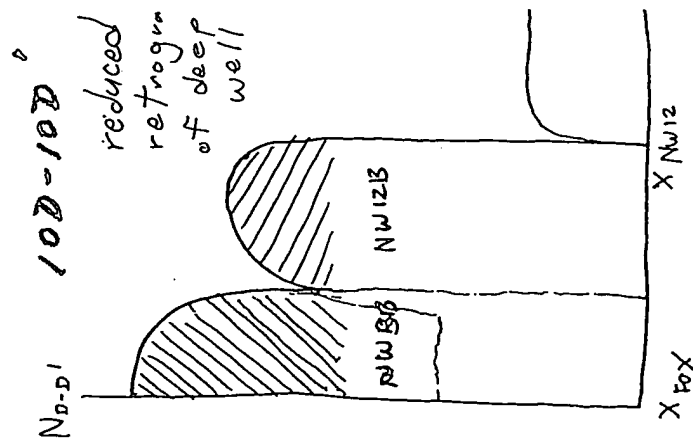


Fig. 10J

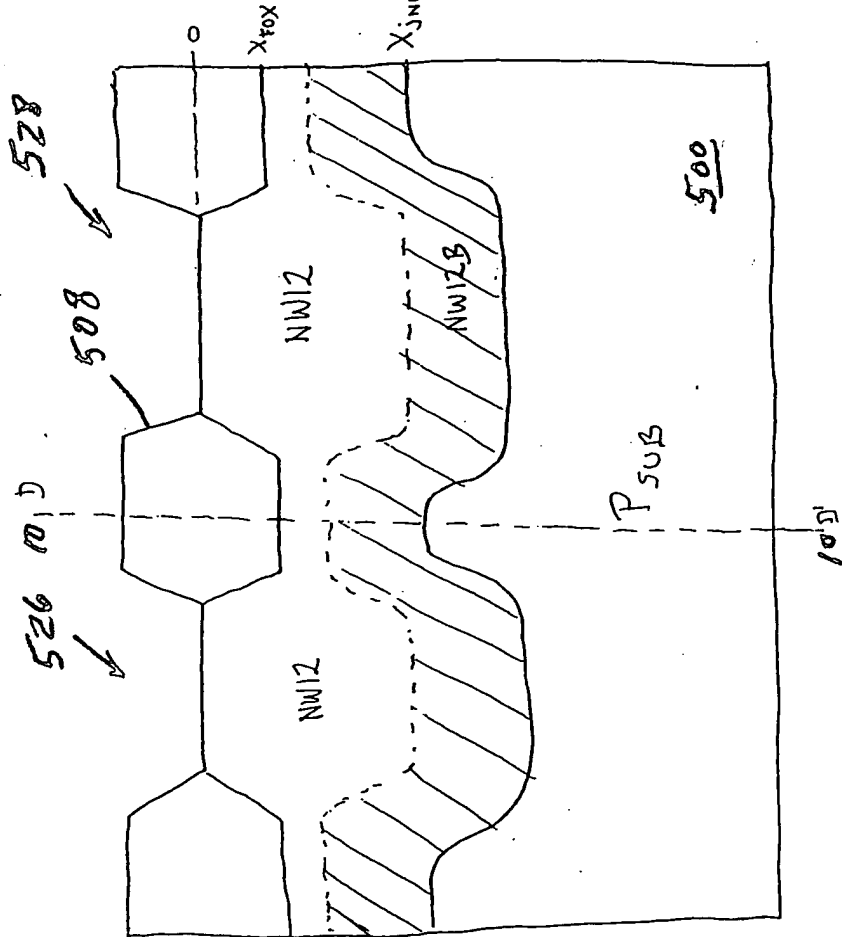
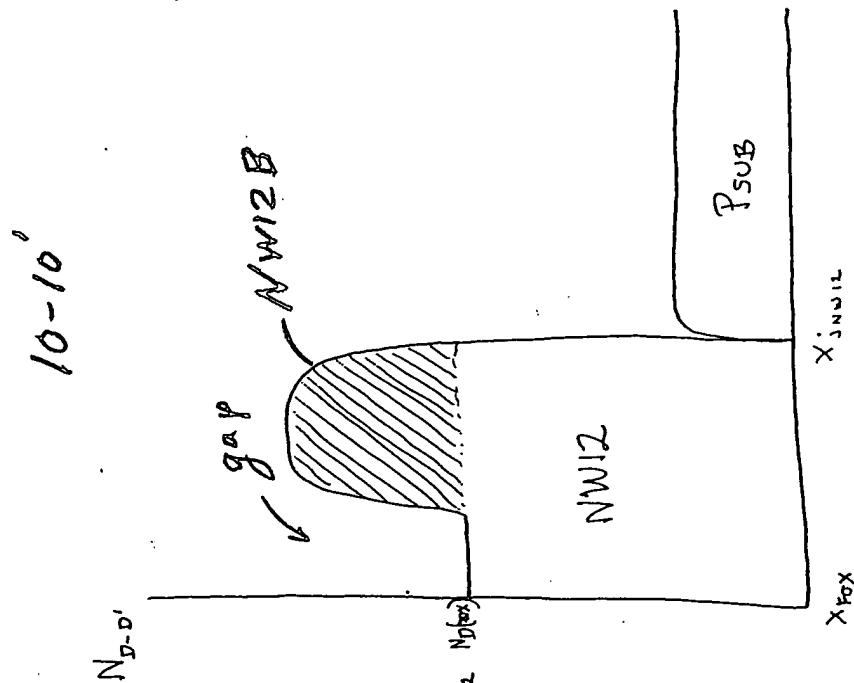


Fig. 10K



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Fig. 10L

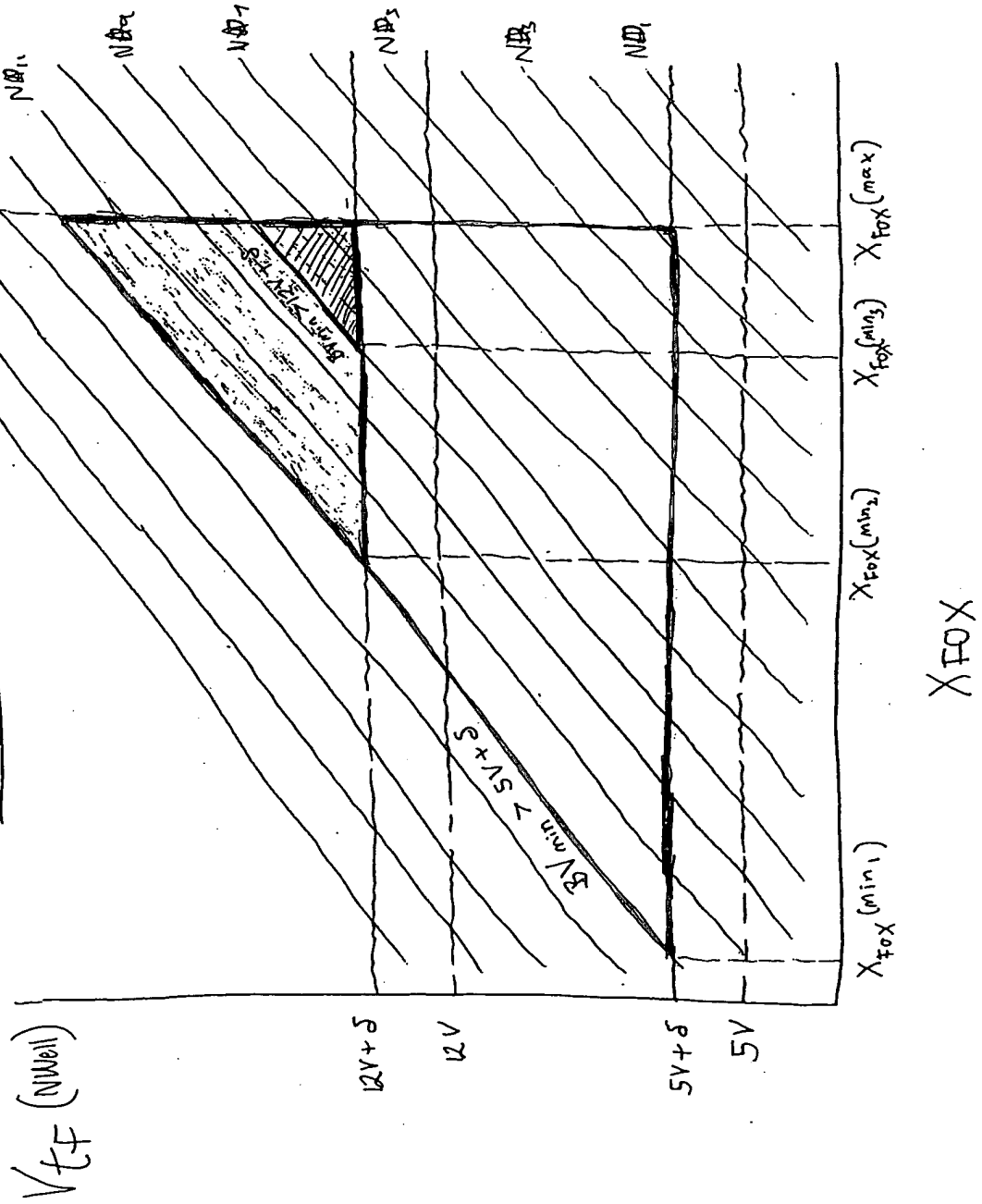


Fig. 11A

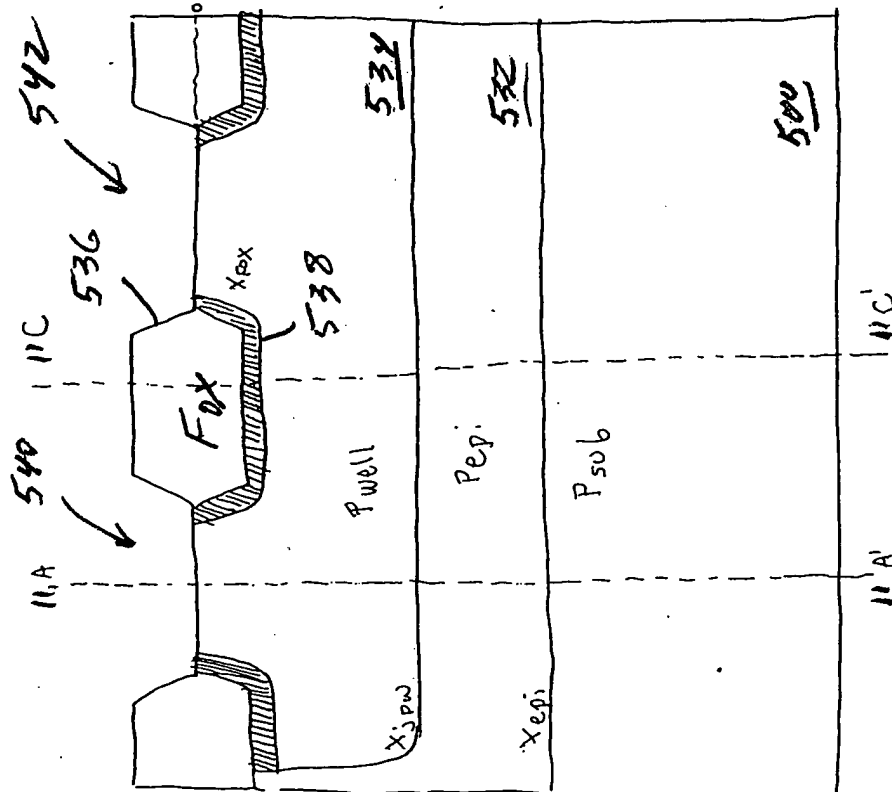


Fig. 11B

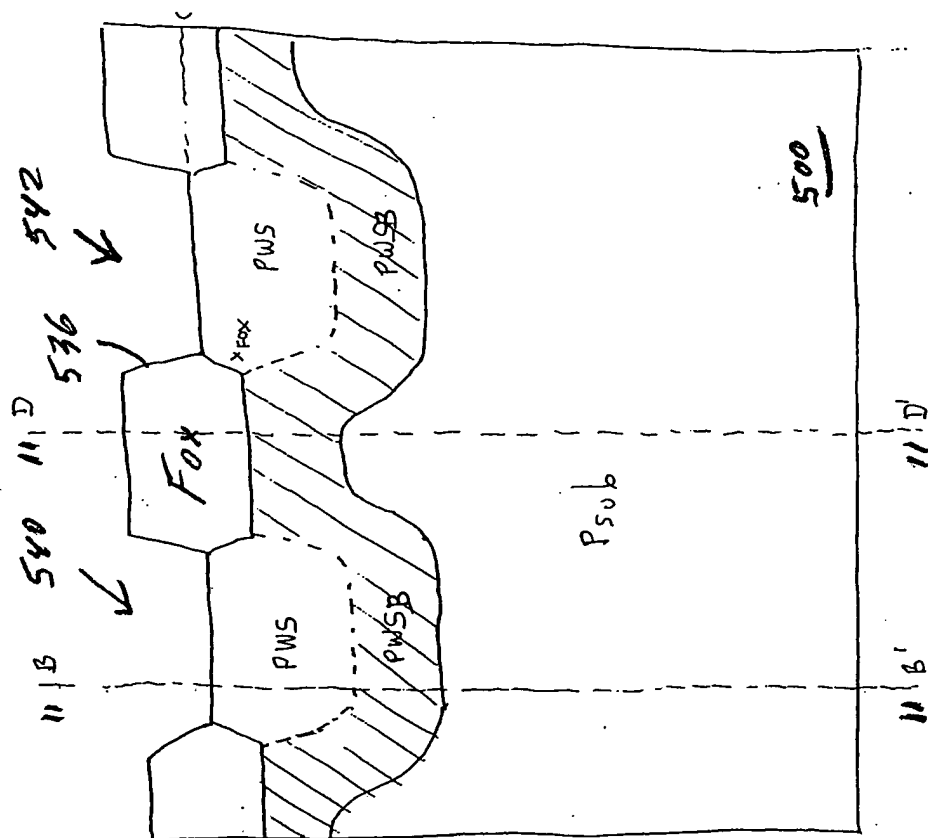


Fig. 11C

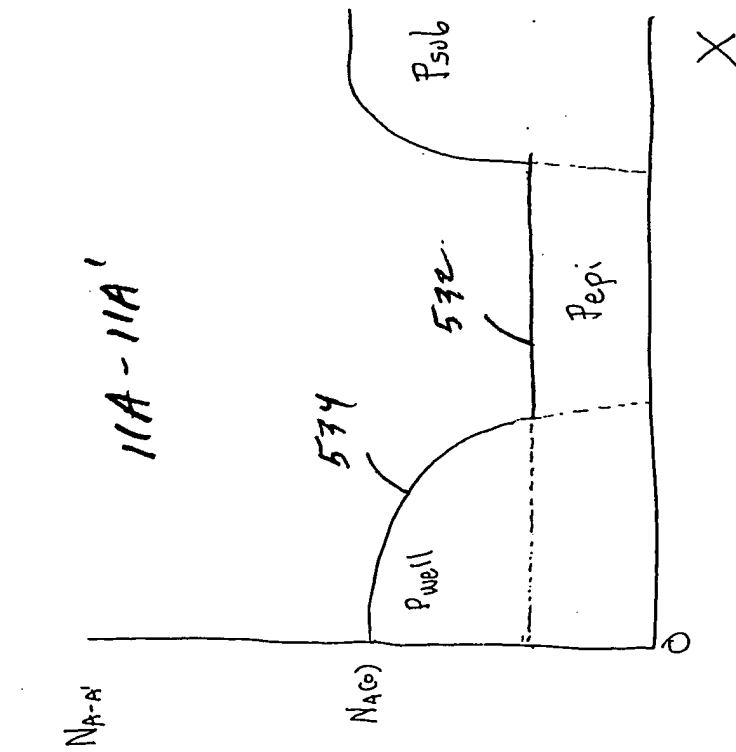


Fig. 11D

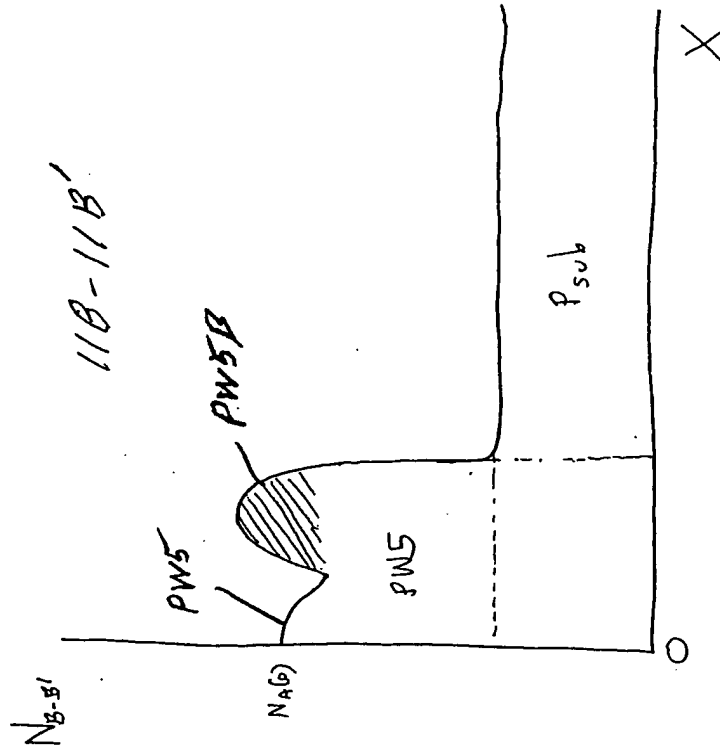




Fig. 11F

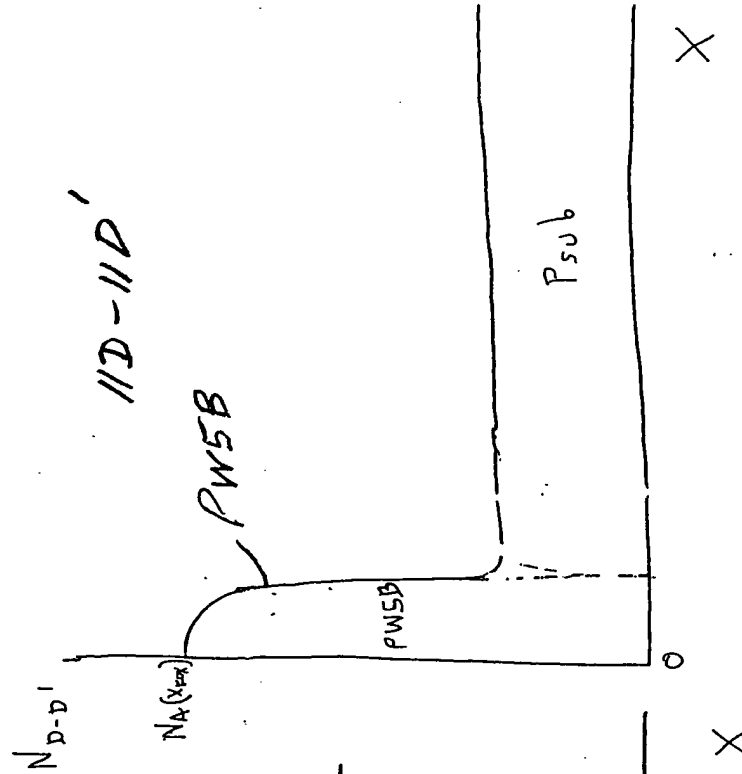


Fig. 11E

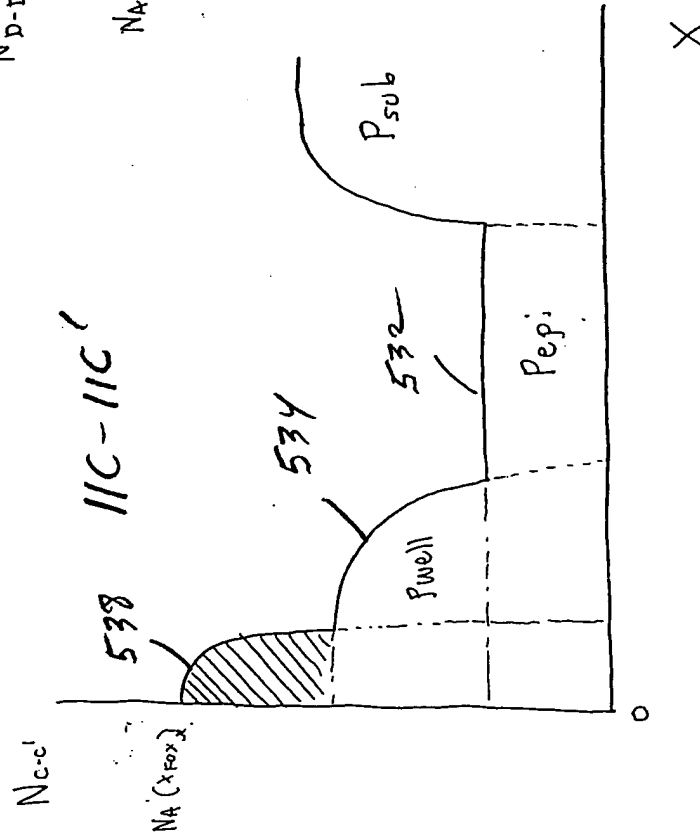


Fig. 11H

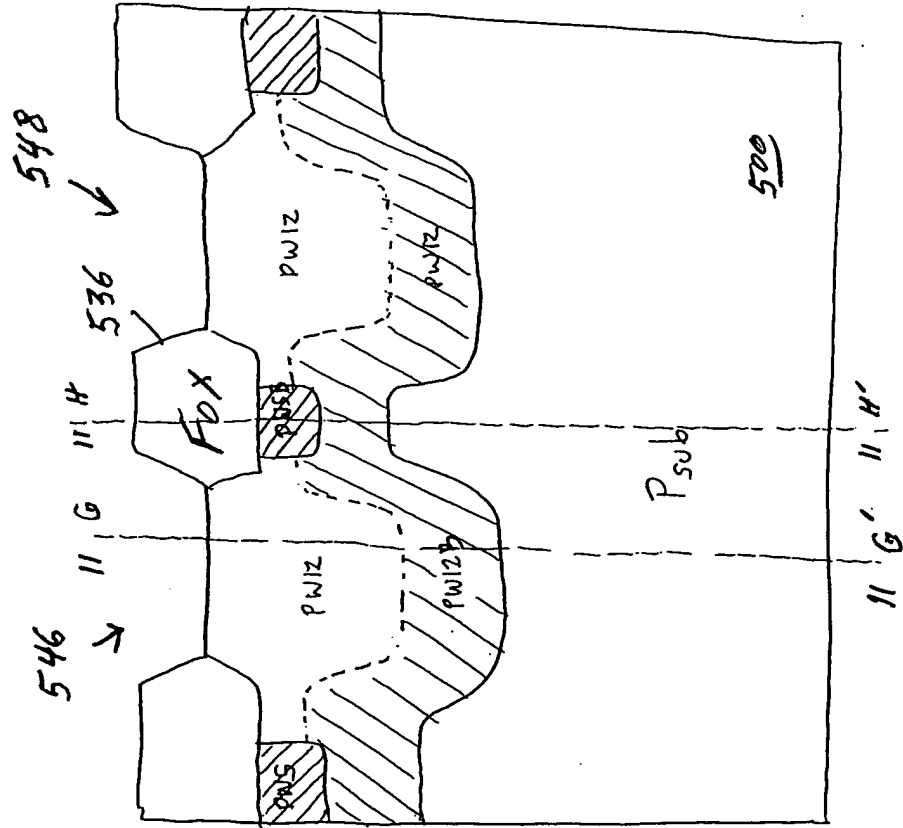


Fig. 11G

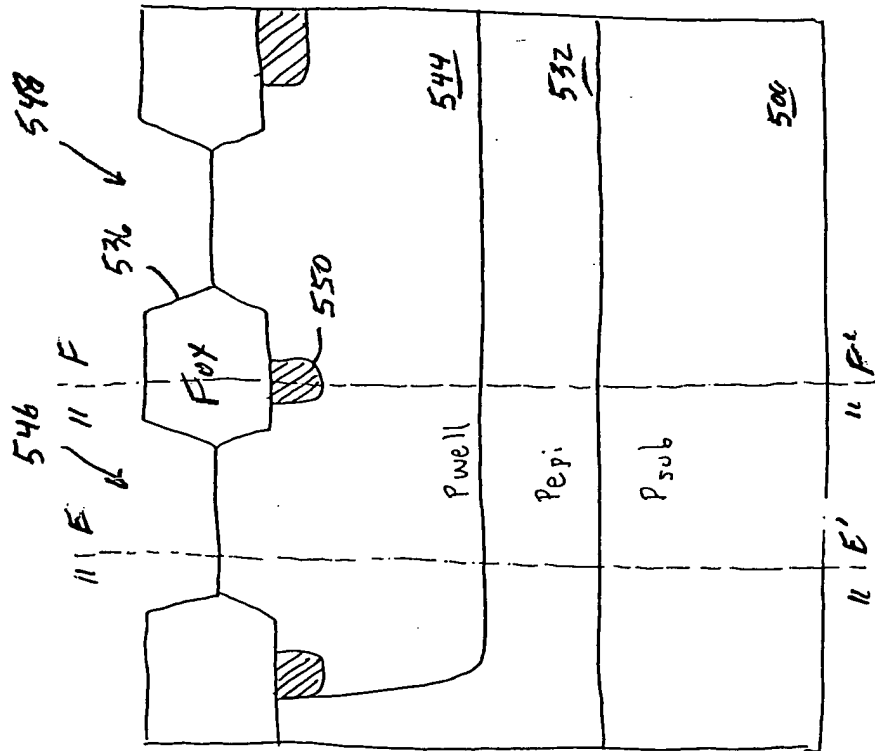
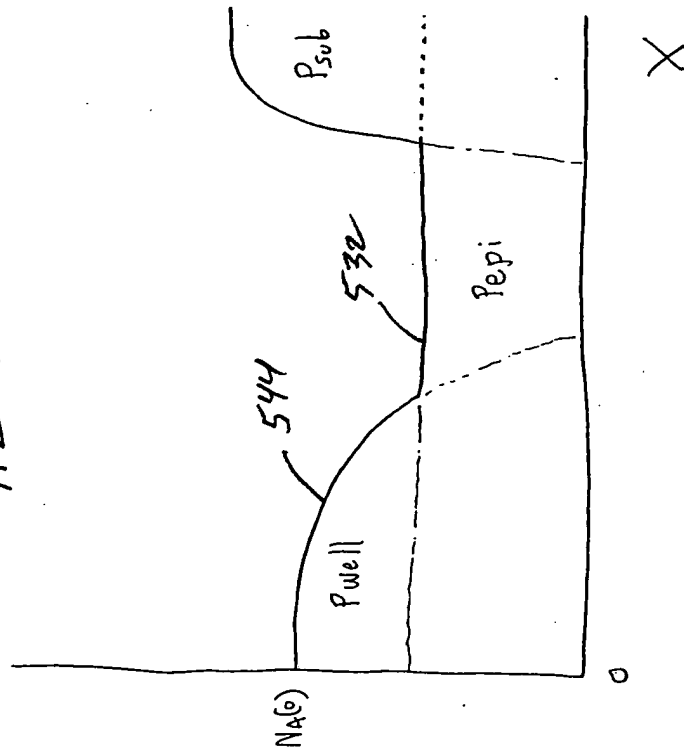


Fig. 11I

11E-11E'

Fig. 11J

11G-11G'

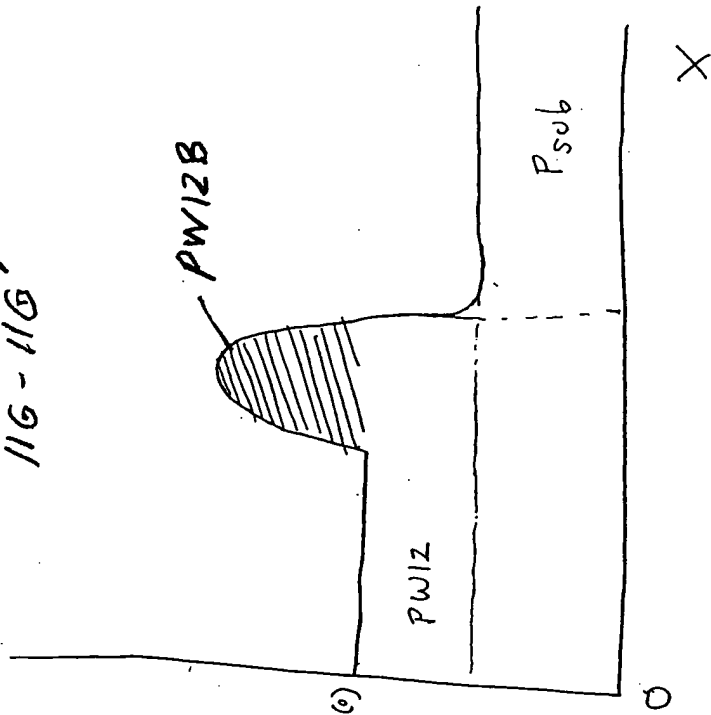


Fig. 11K

11F-11F'

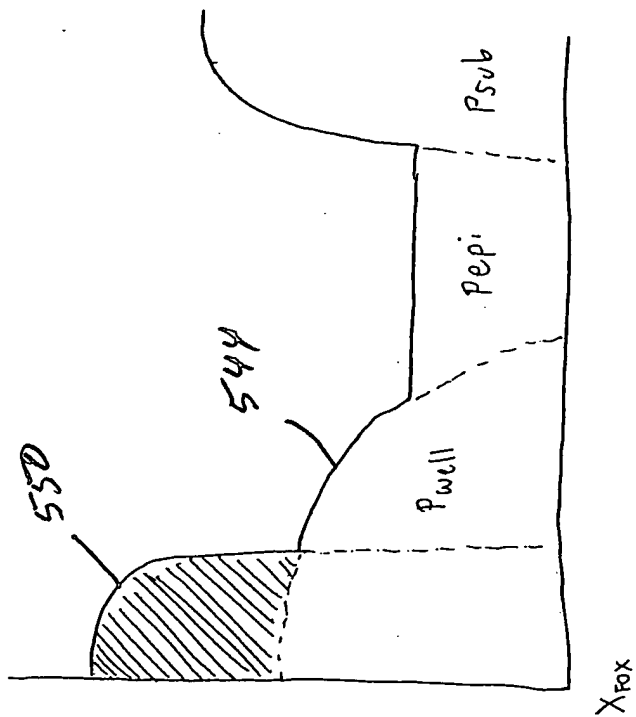


Fig. 11L

11H-11H'

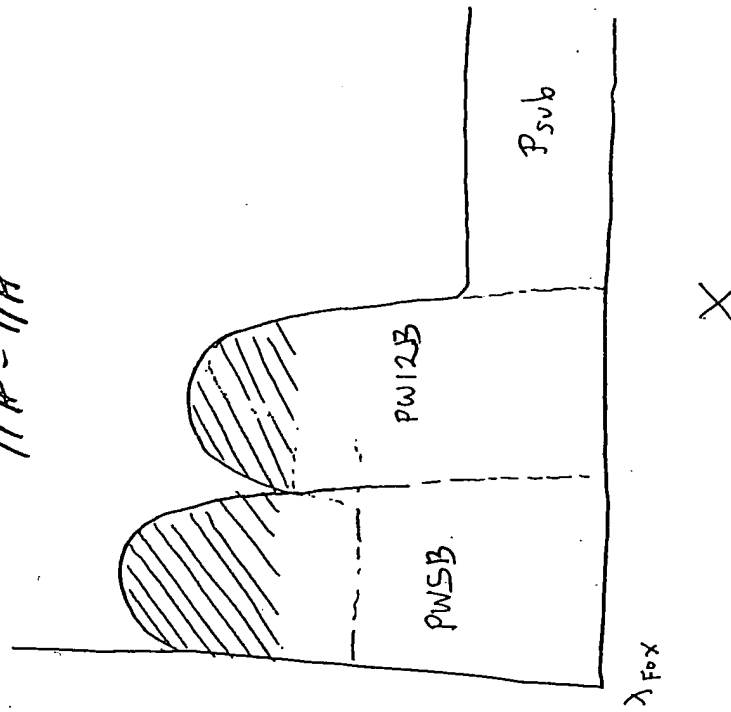


Fig. 12A  
epitaxial

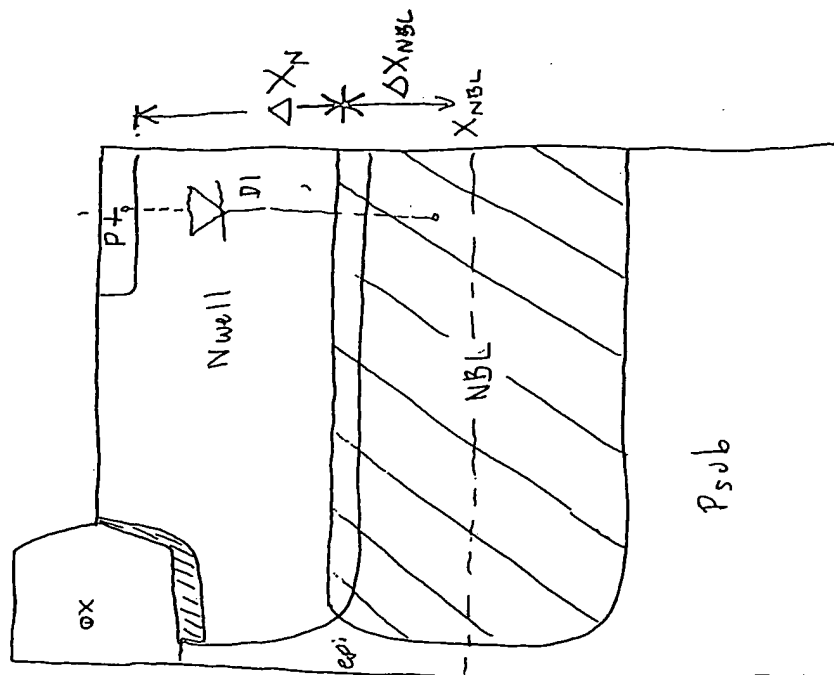


Fig. 12B

implanted

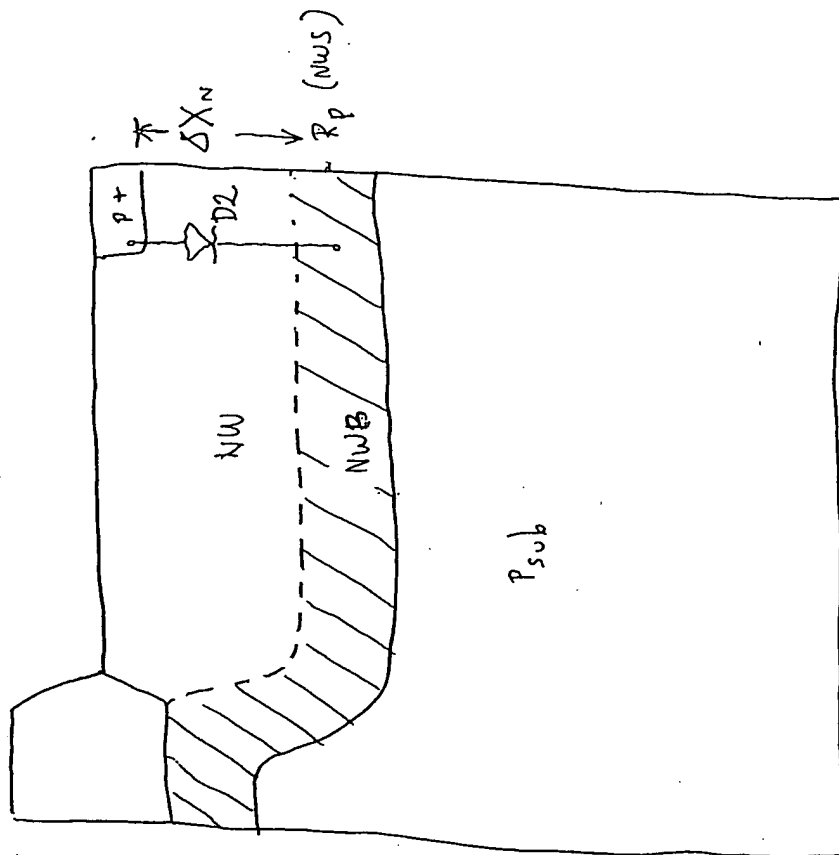


Fig. 12C

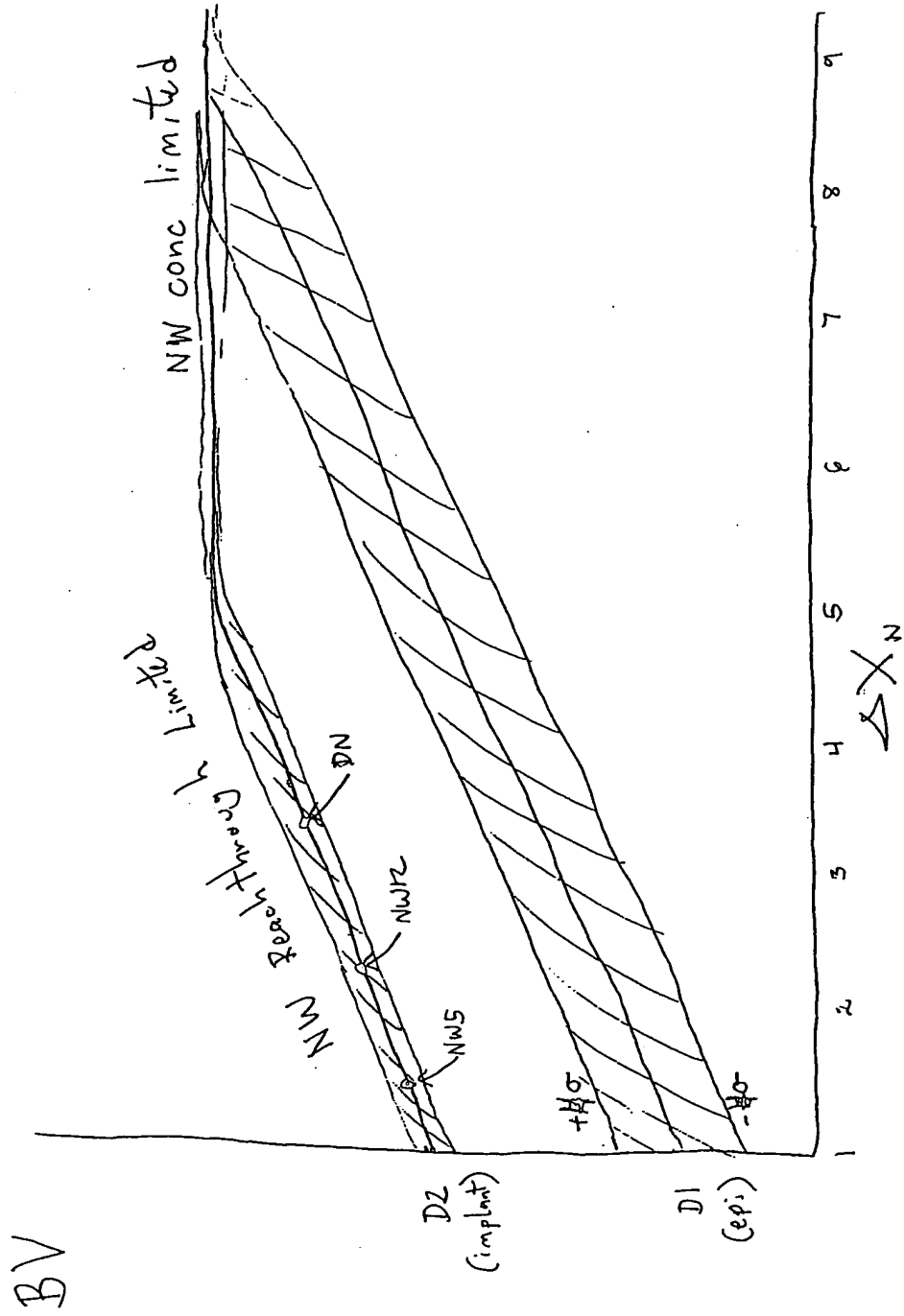


Fig. 3A

Prior Art

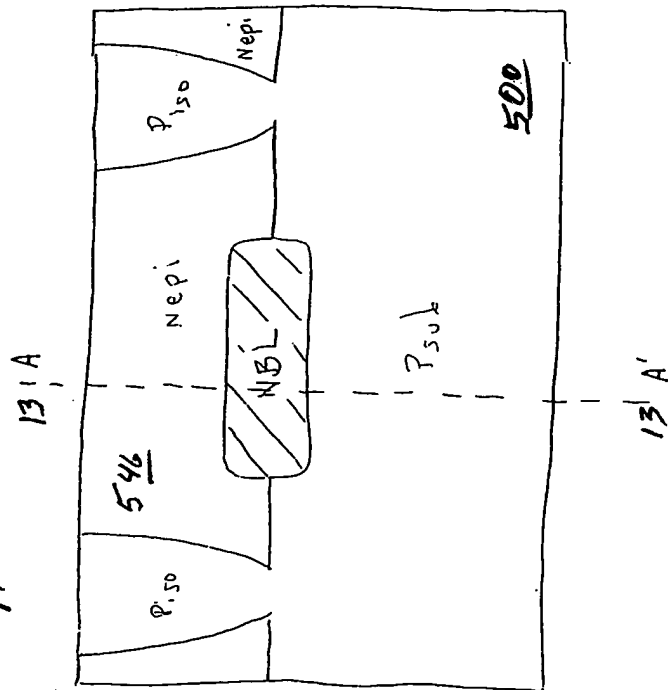


Fig. 3B

Prior Art

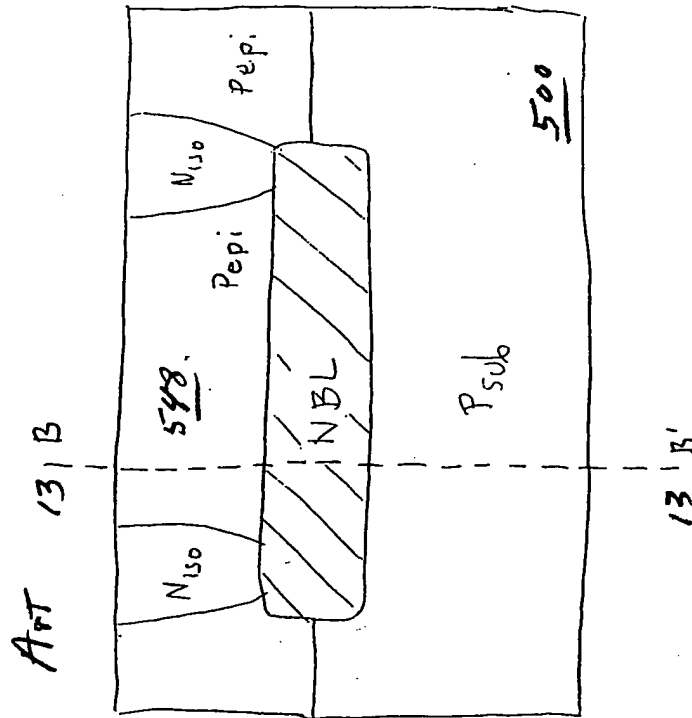


Fig 13C

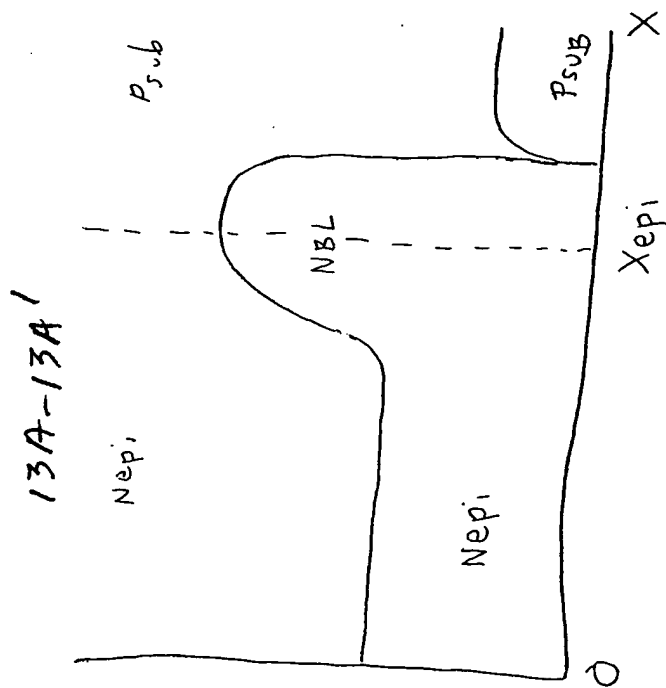


Fig 13D

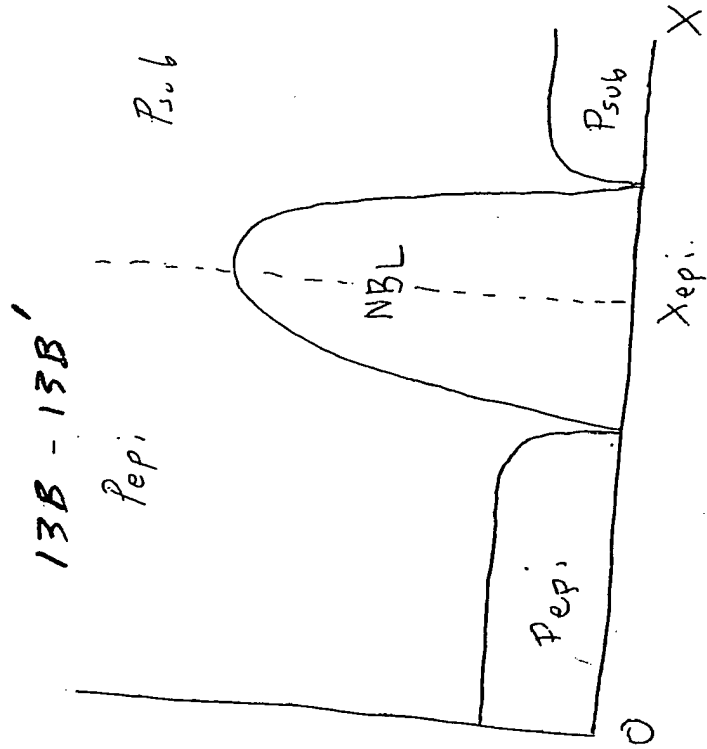




Fig. 13G

13C-13C'

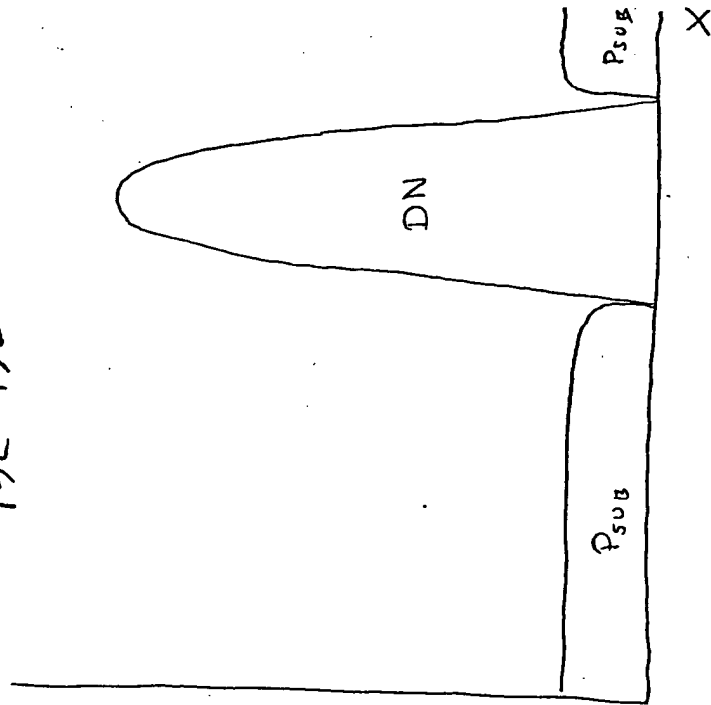
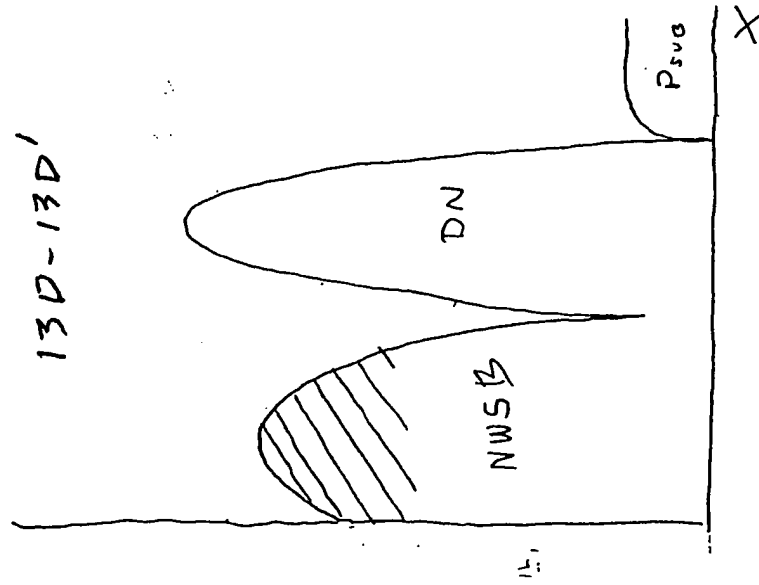


Fig. 13H

13D-13D'



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Fig. 13E

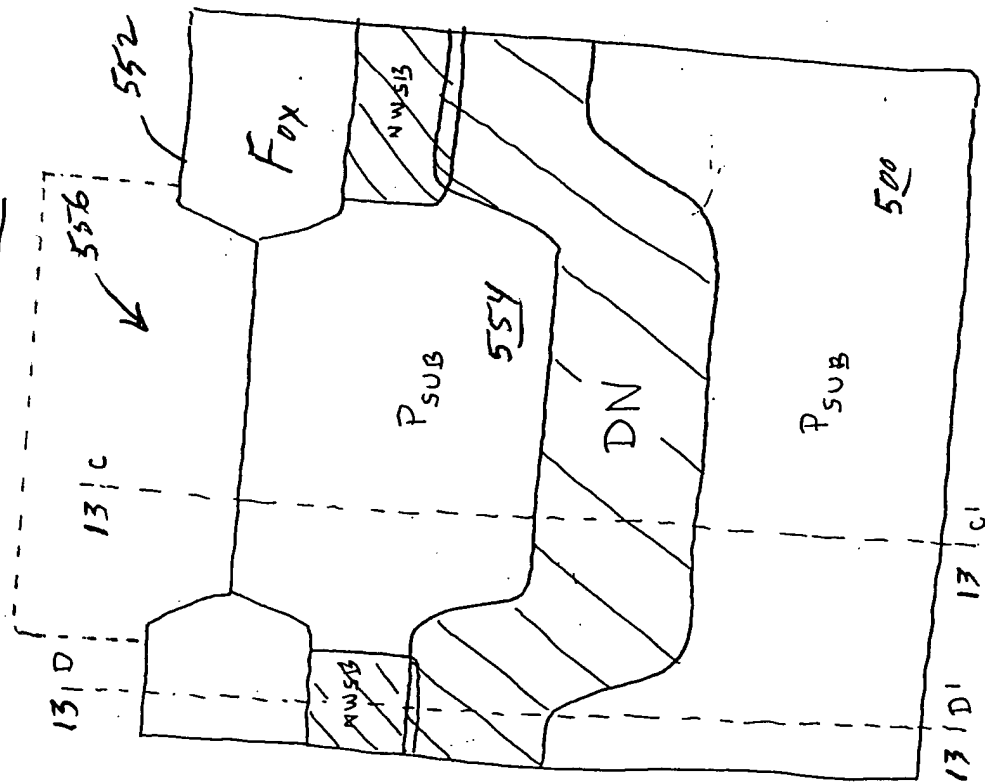


Fig. 13F

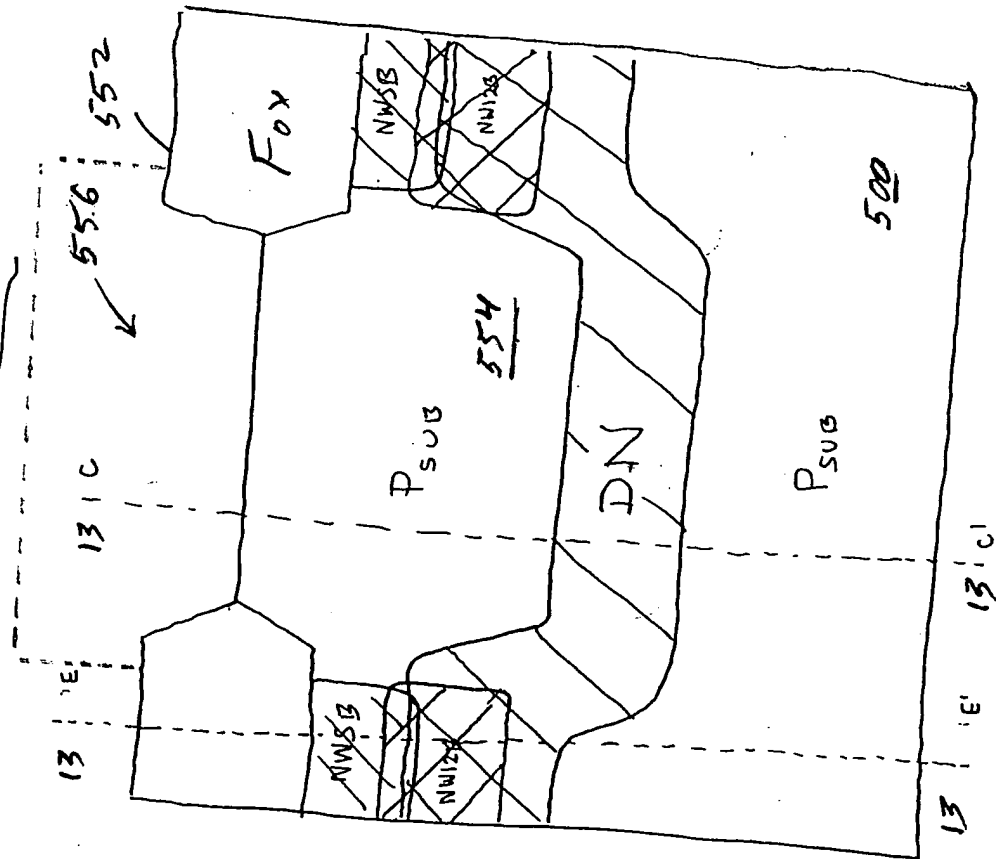


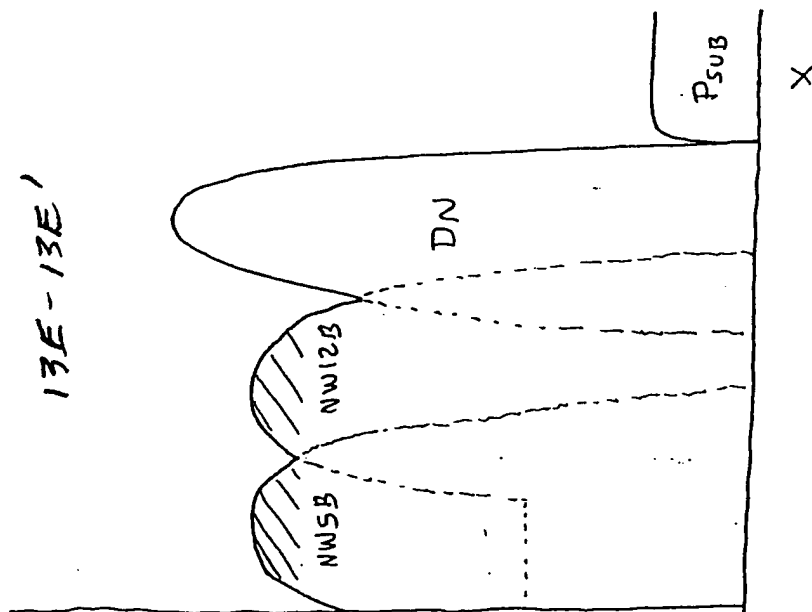
Fig. 13I

Fig 14A

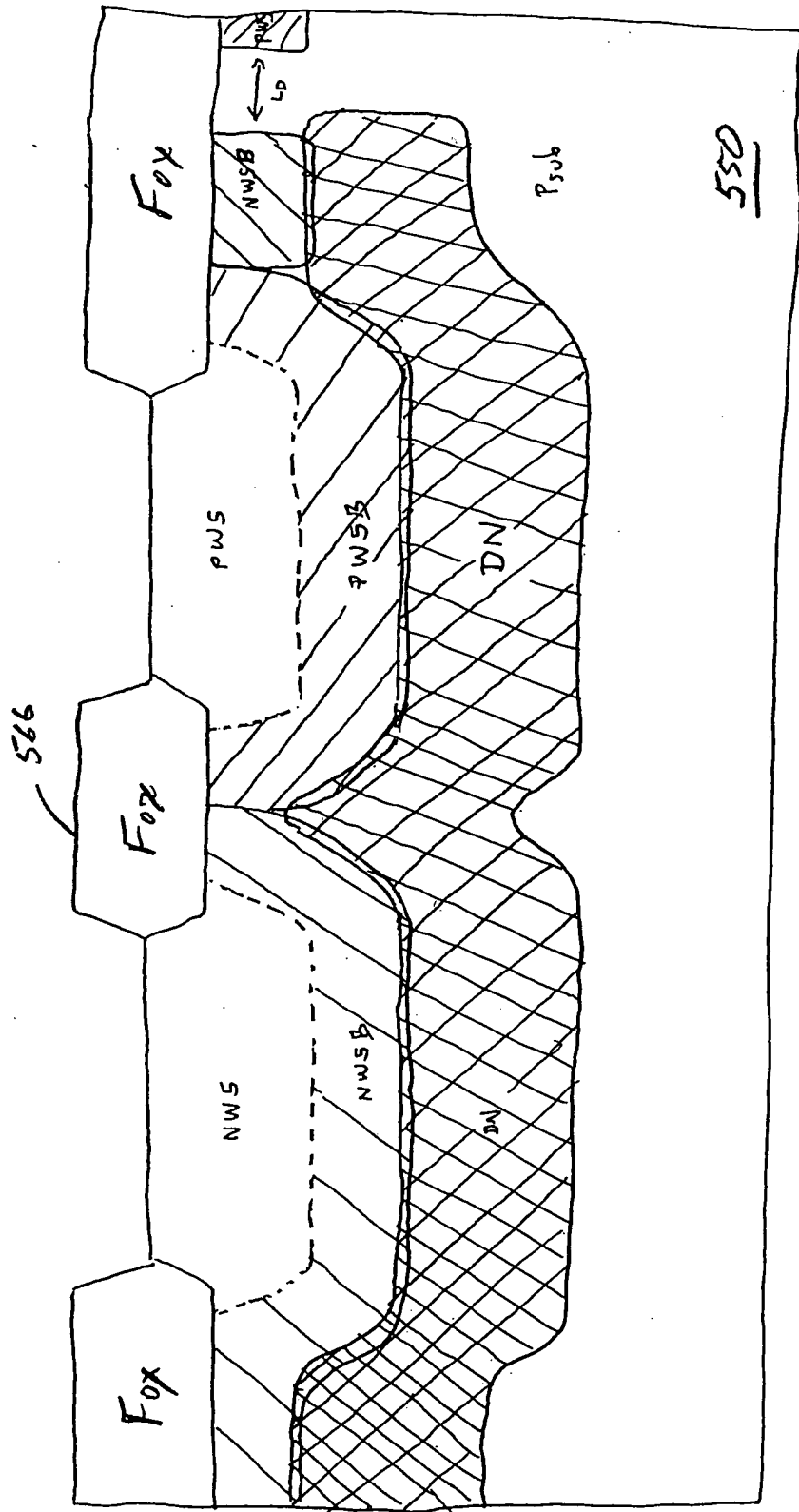


Fig. 14 B.

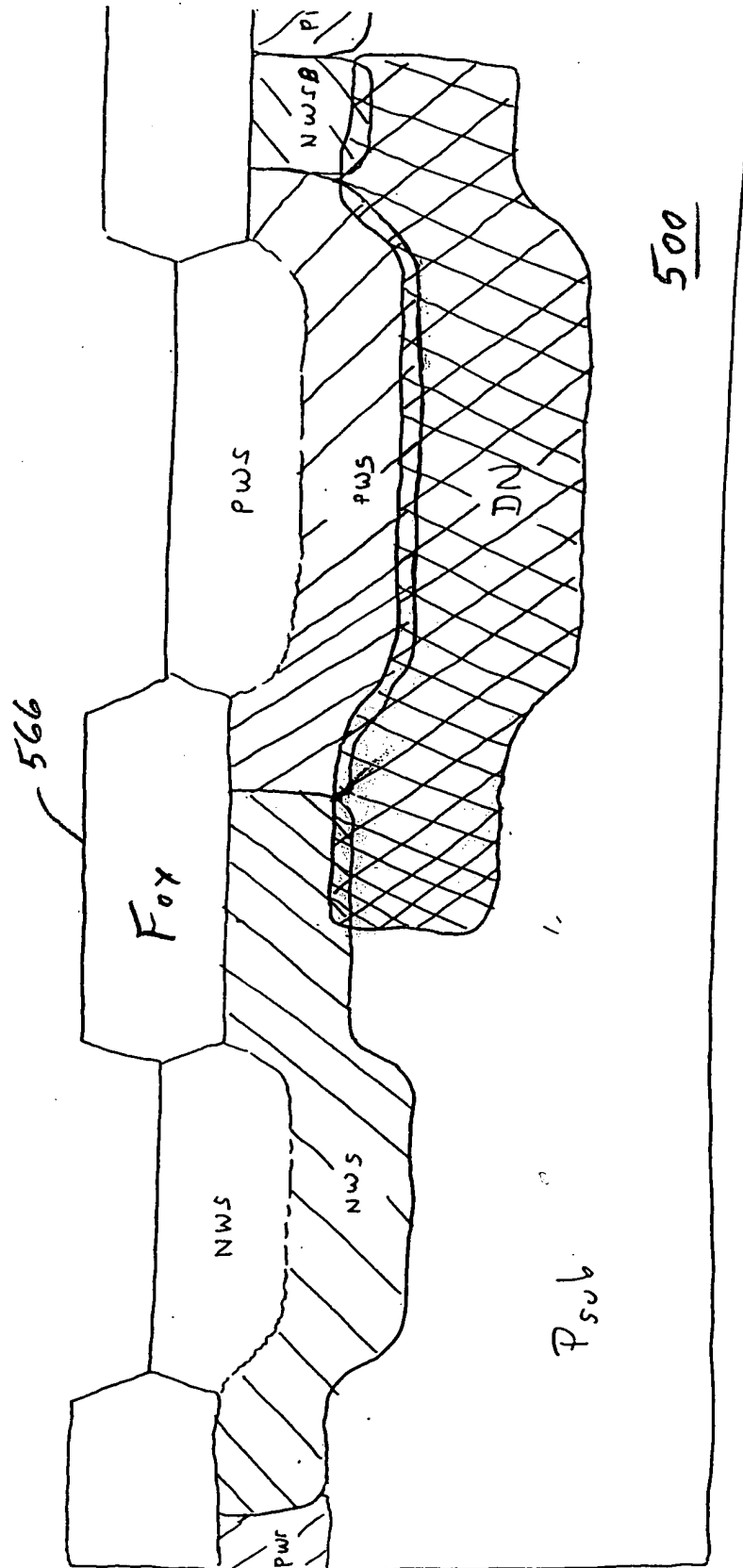
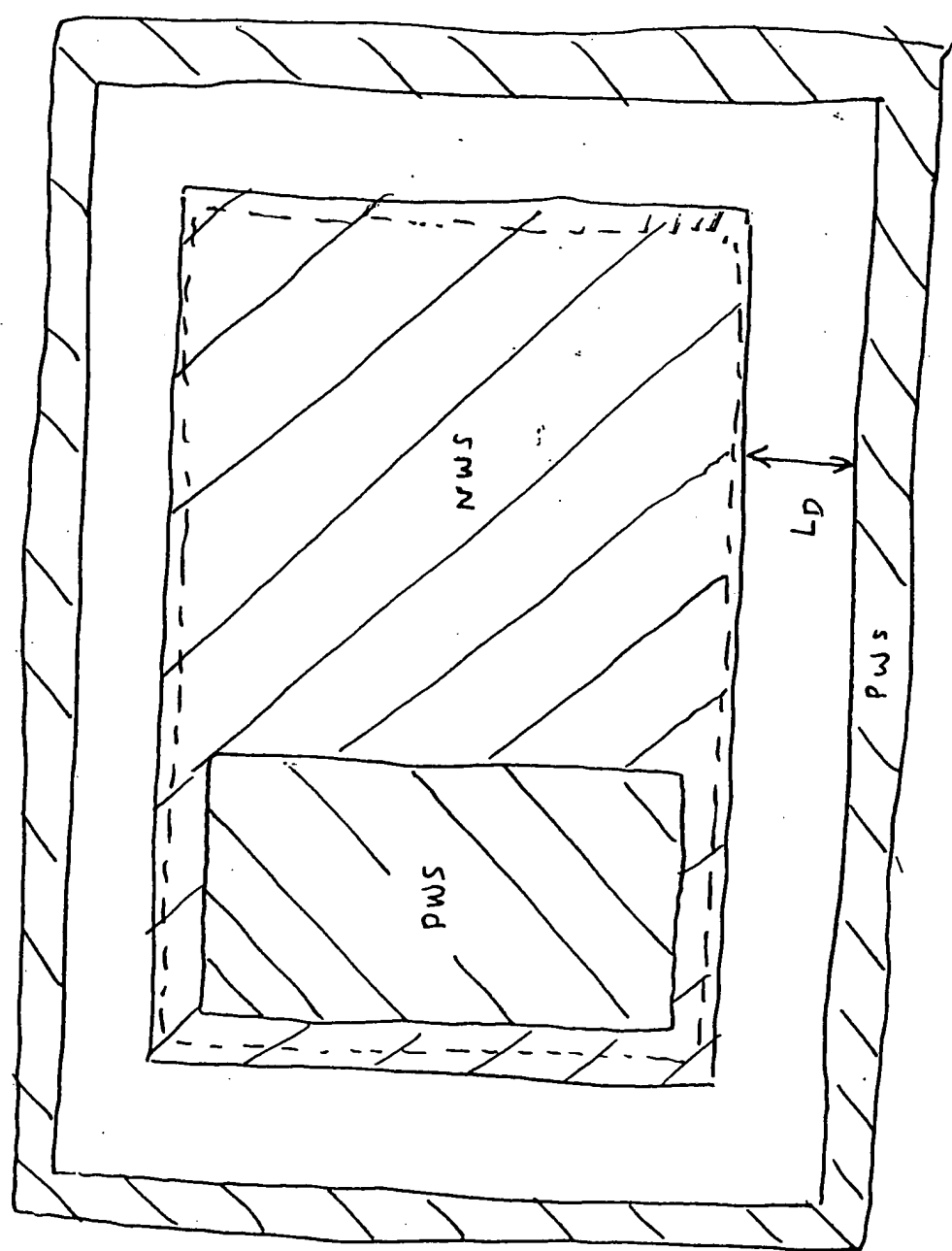


Fig. 14 C



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Fig 14D

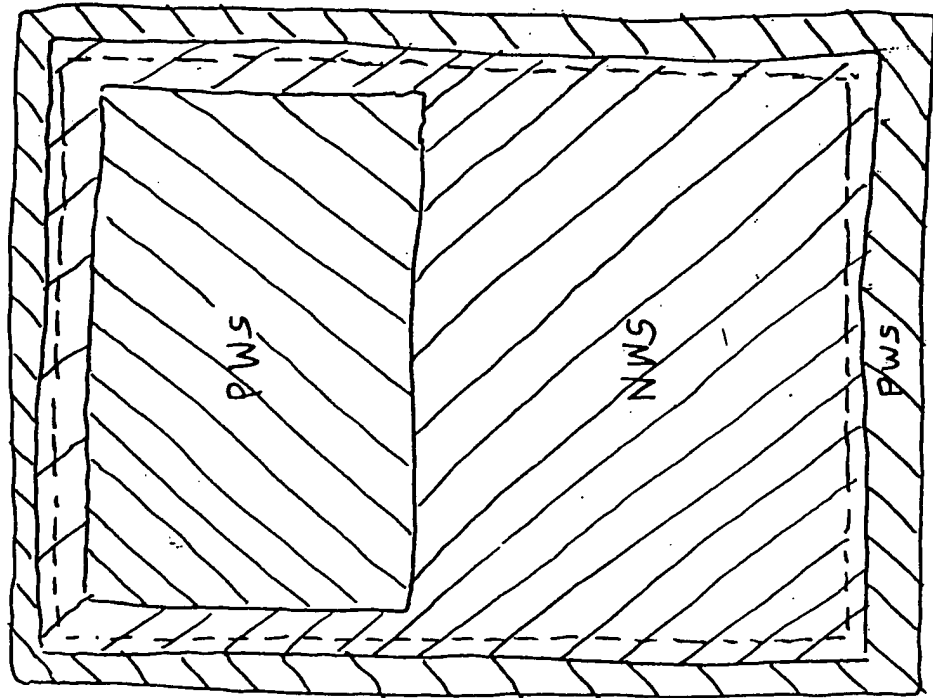


Fig. 14E

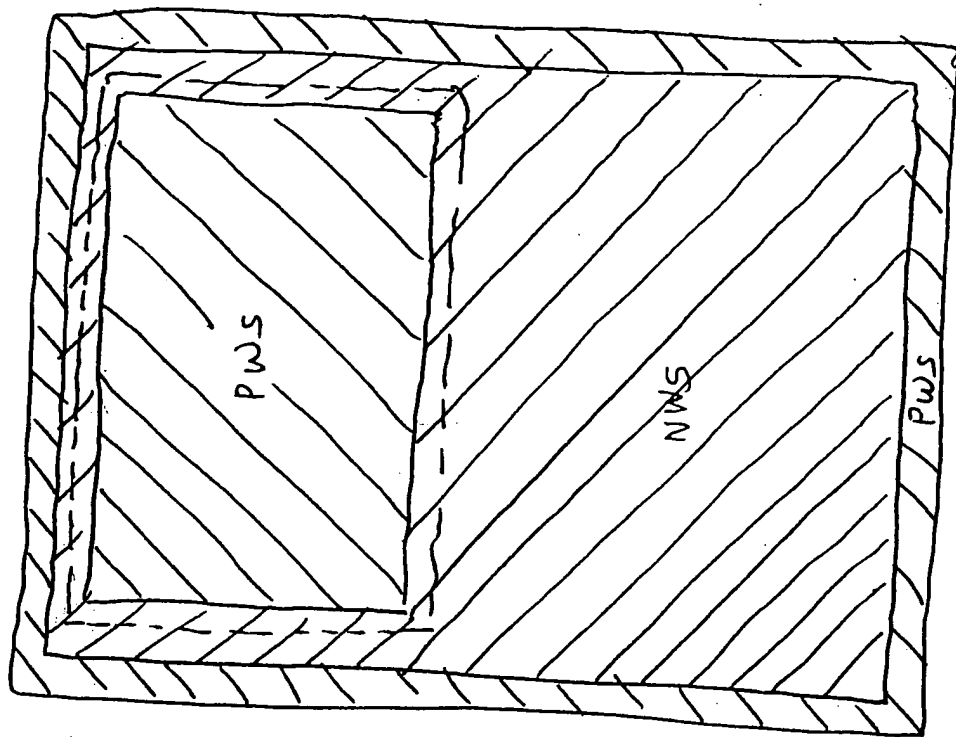


Fig. 14 F

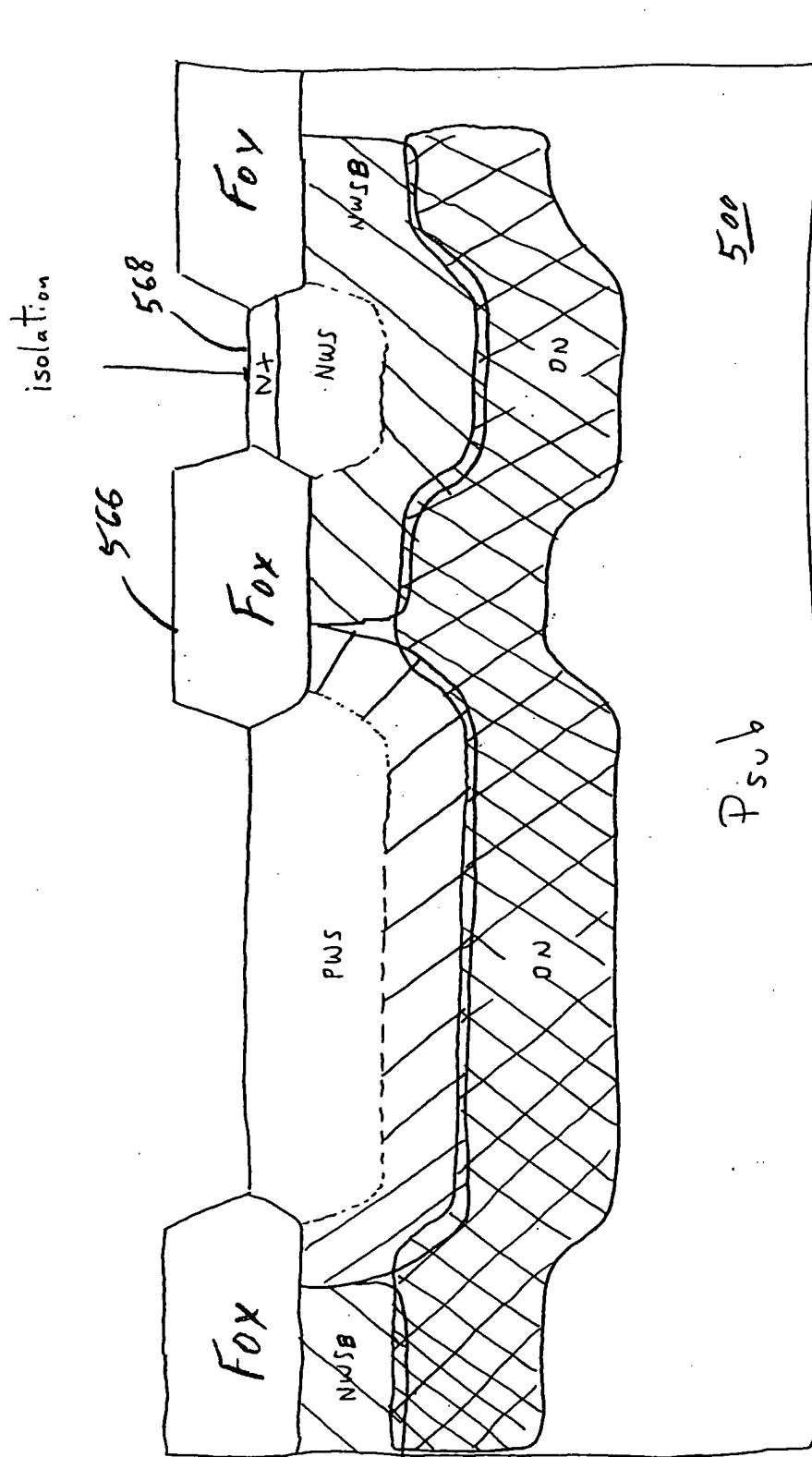




Fig. 146

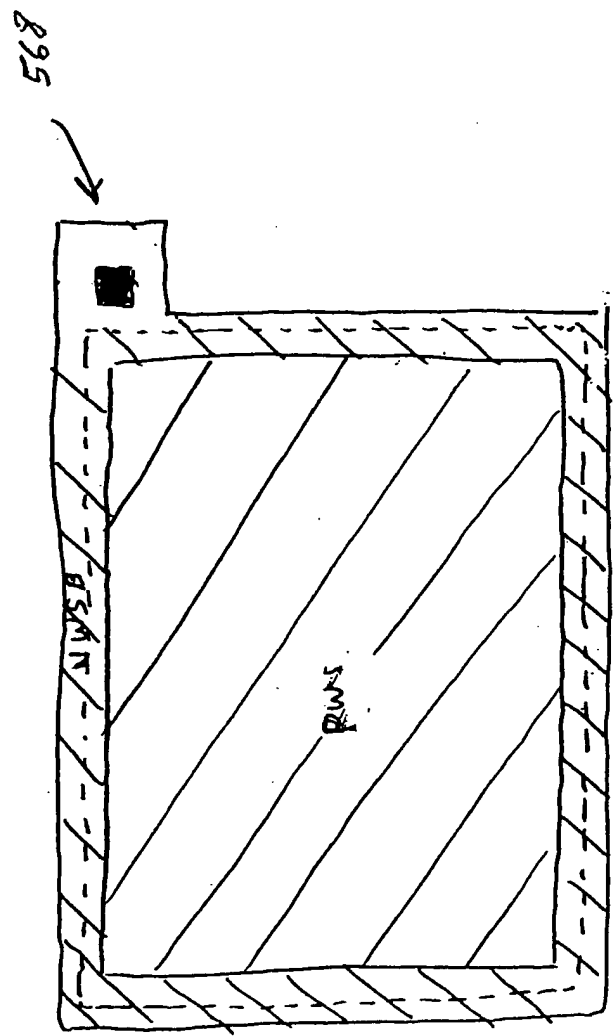


Fig. 14H

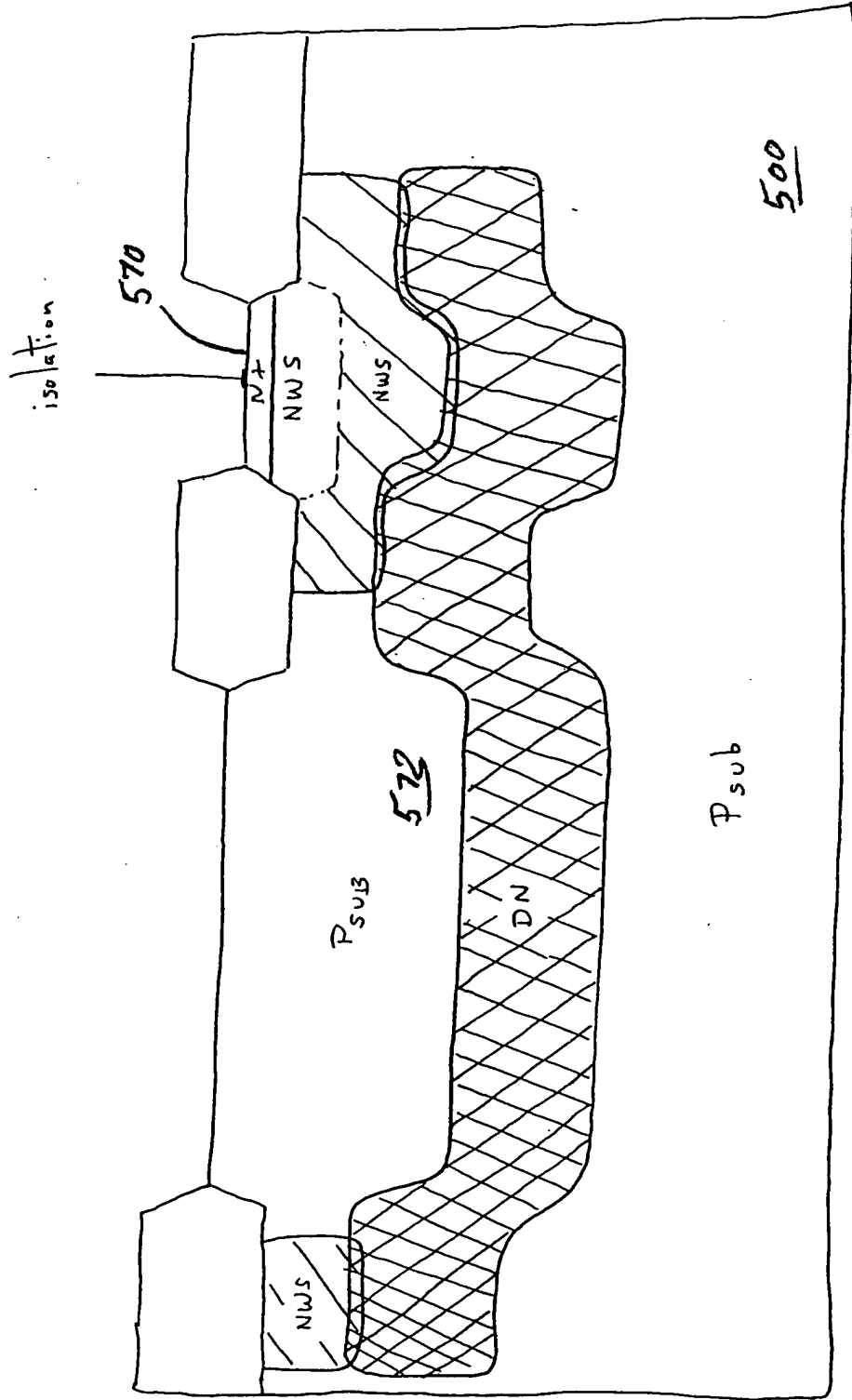


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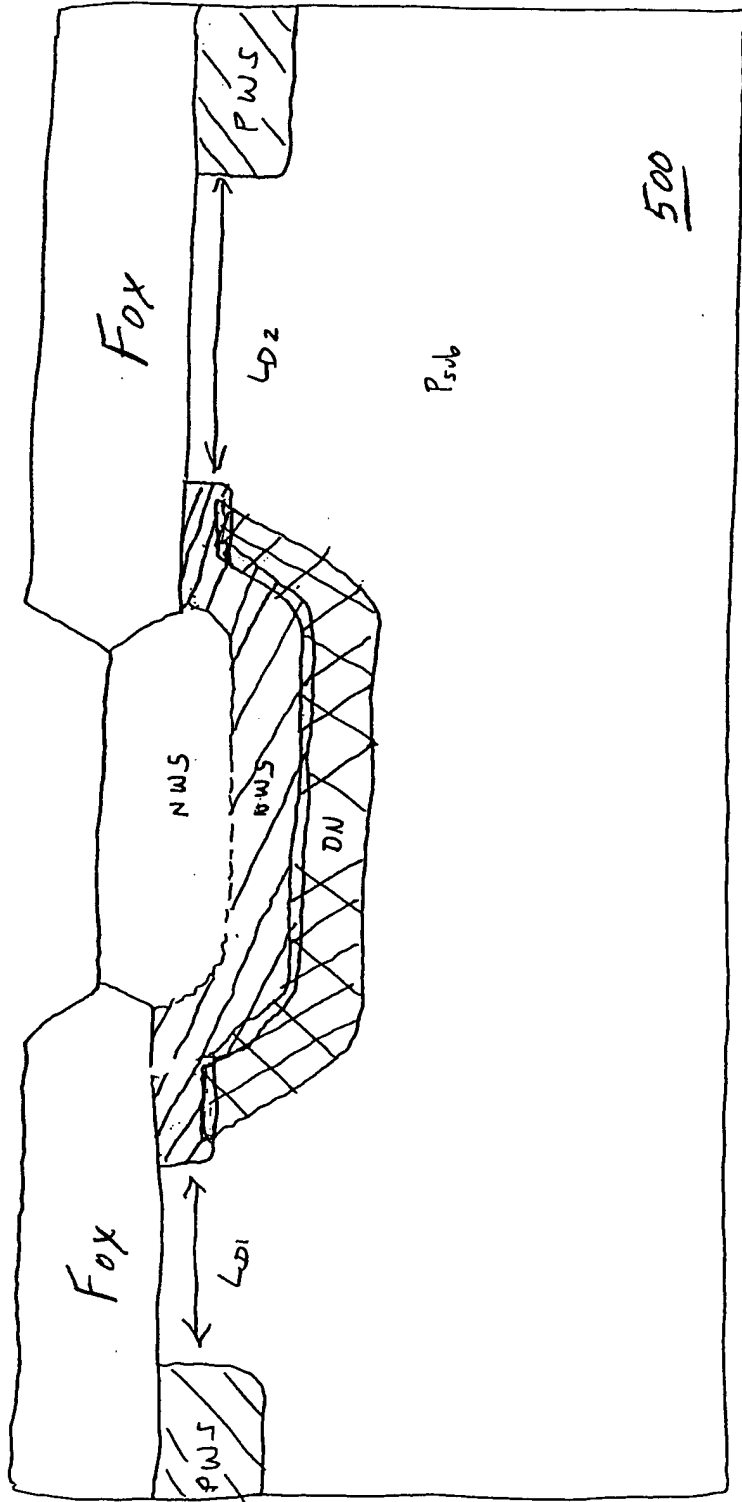
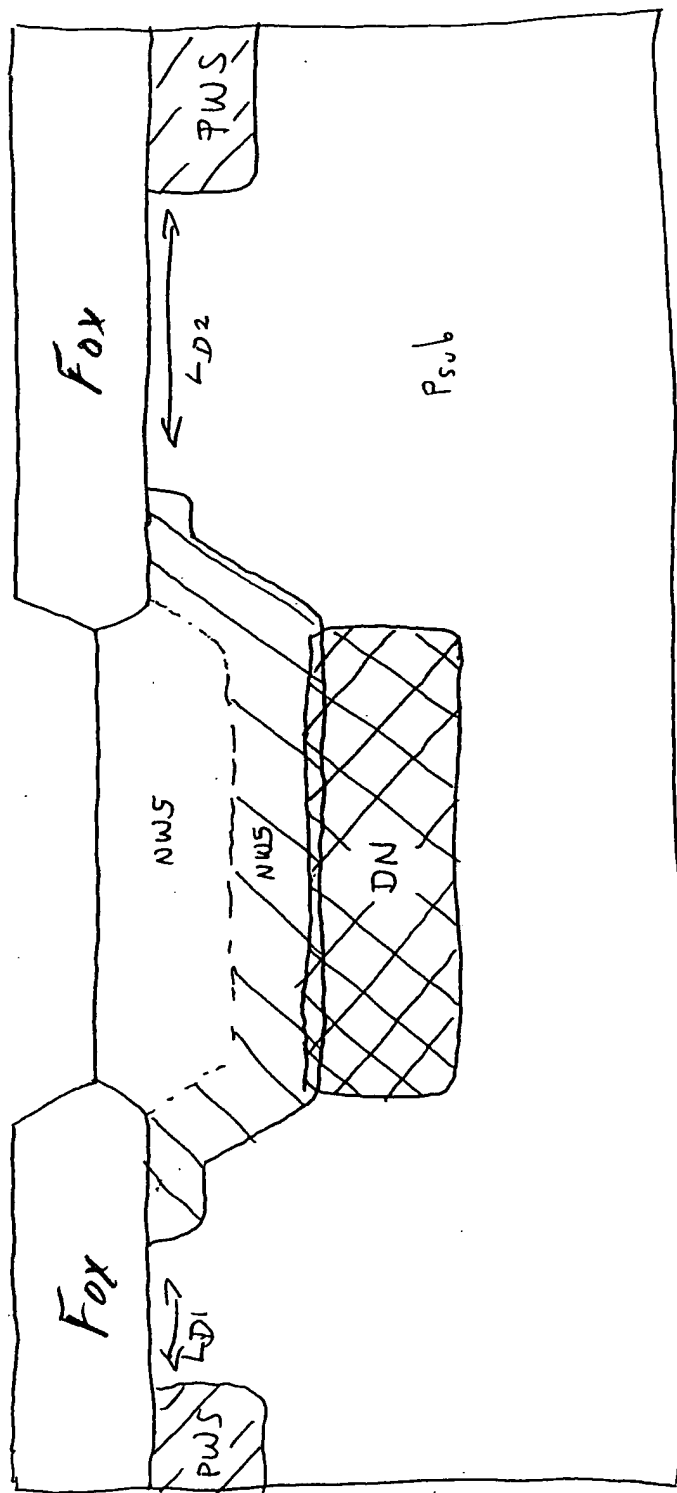


Fig. 14J



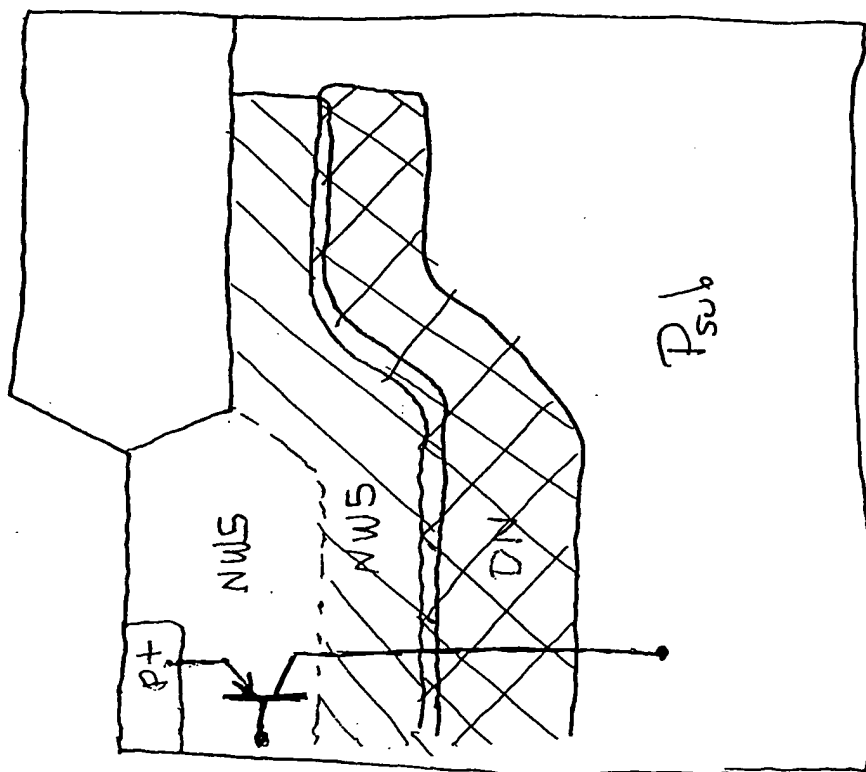


Fig. 14L

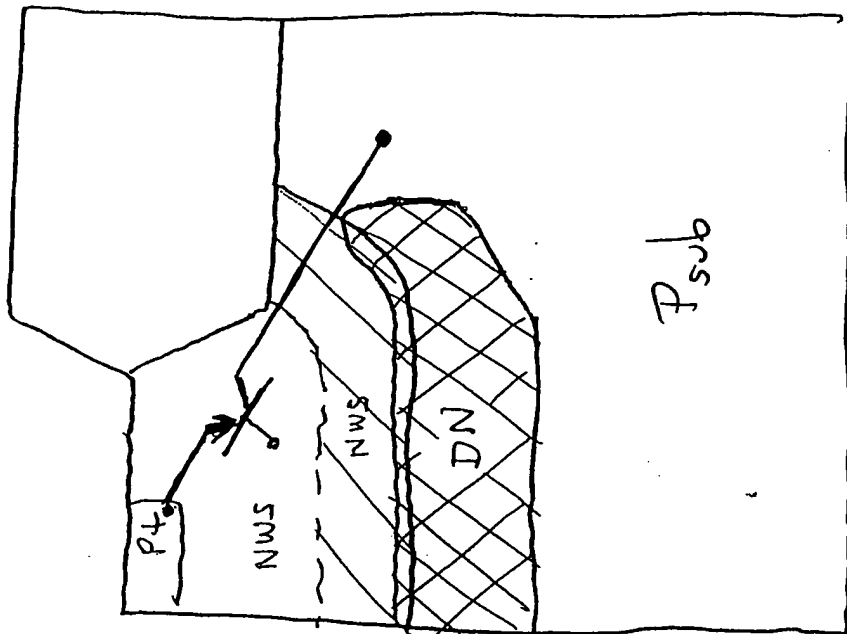


Fig. 14.8

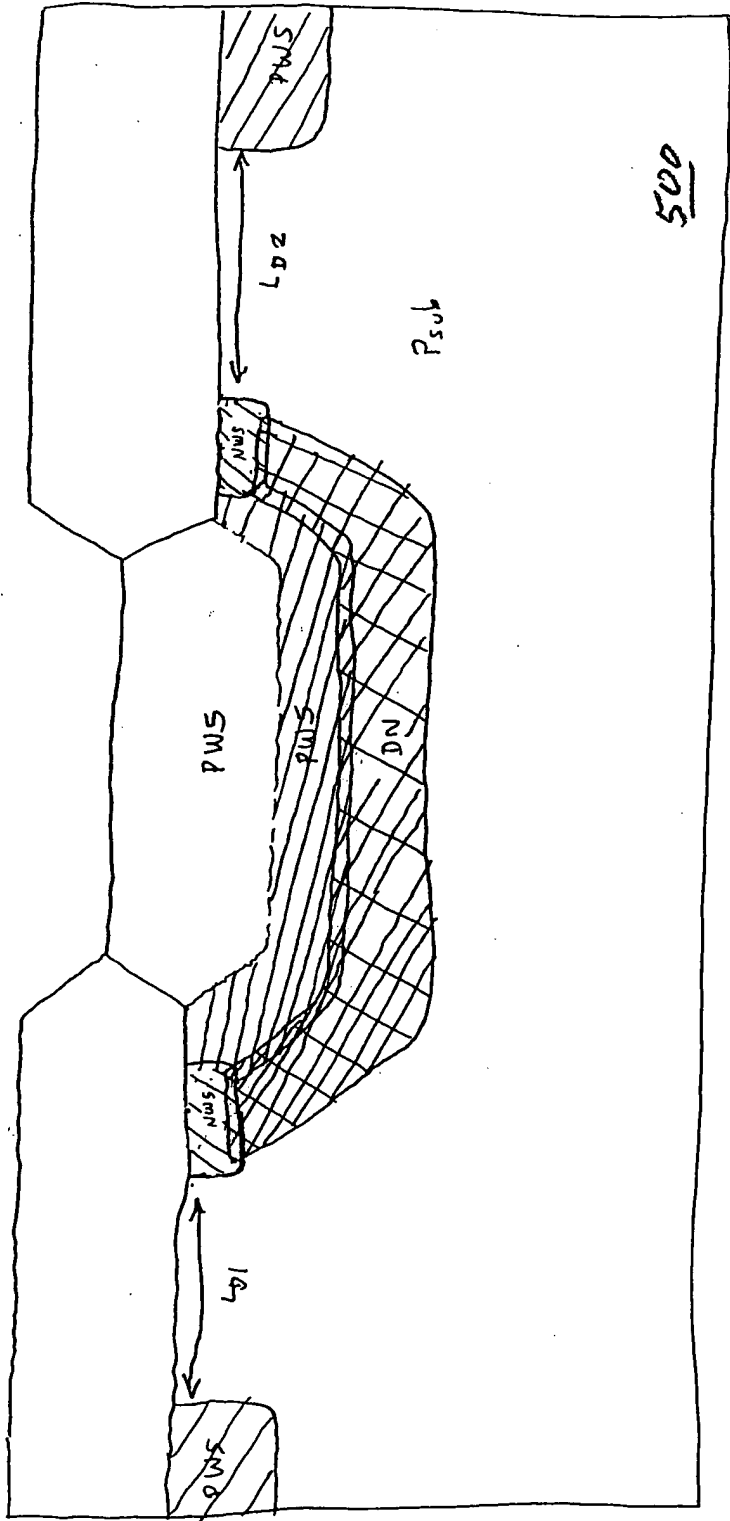


Fig. 14N

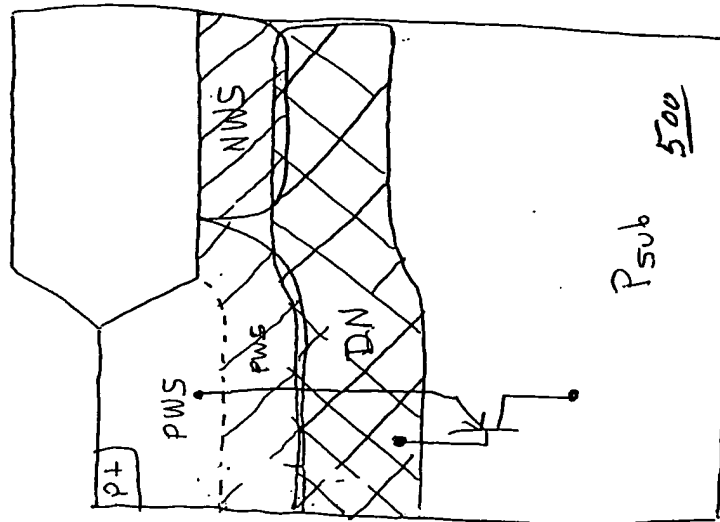


Fig. 14O

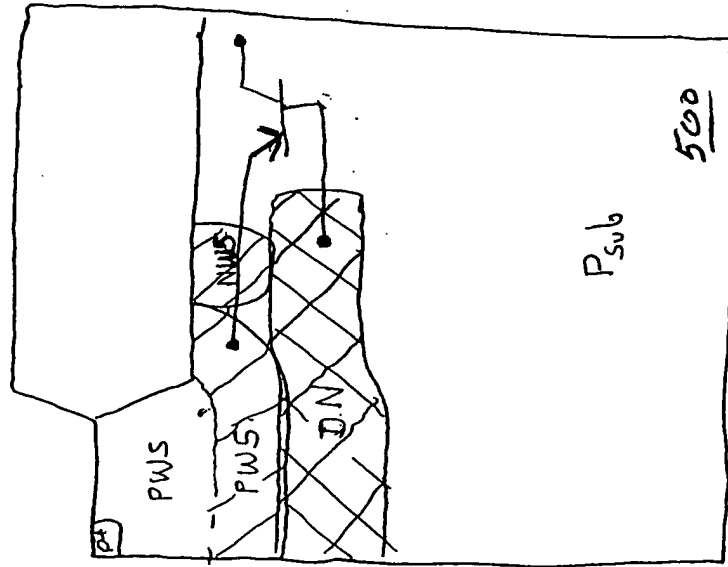


Fig. 14P

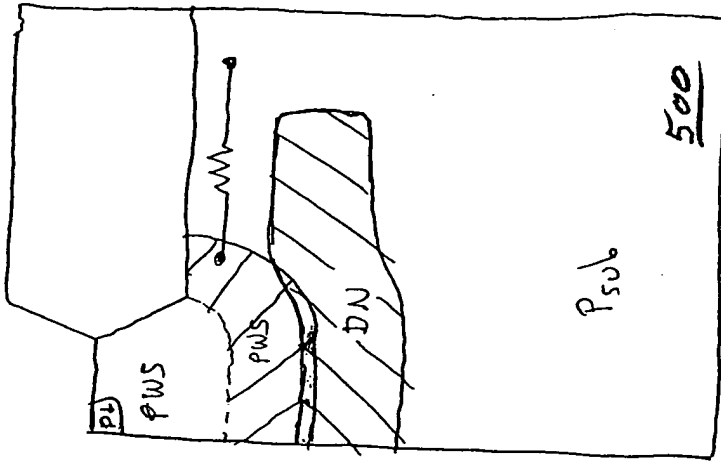


Fig. 15A

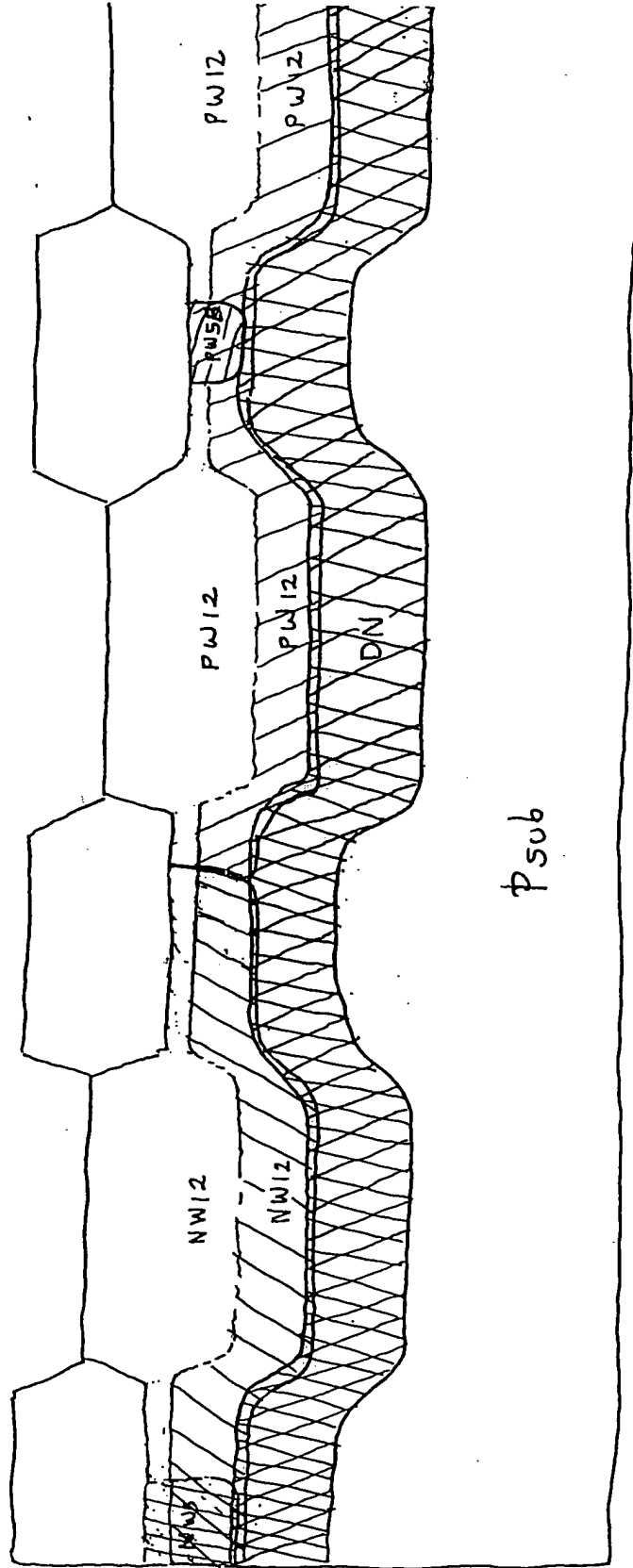






Fig. 15C

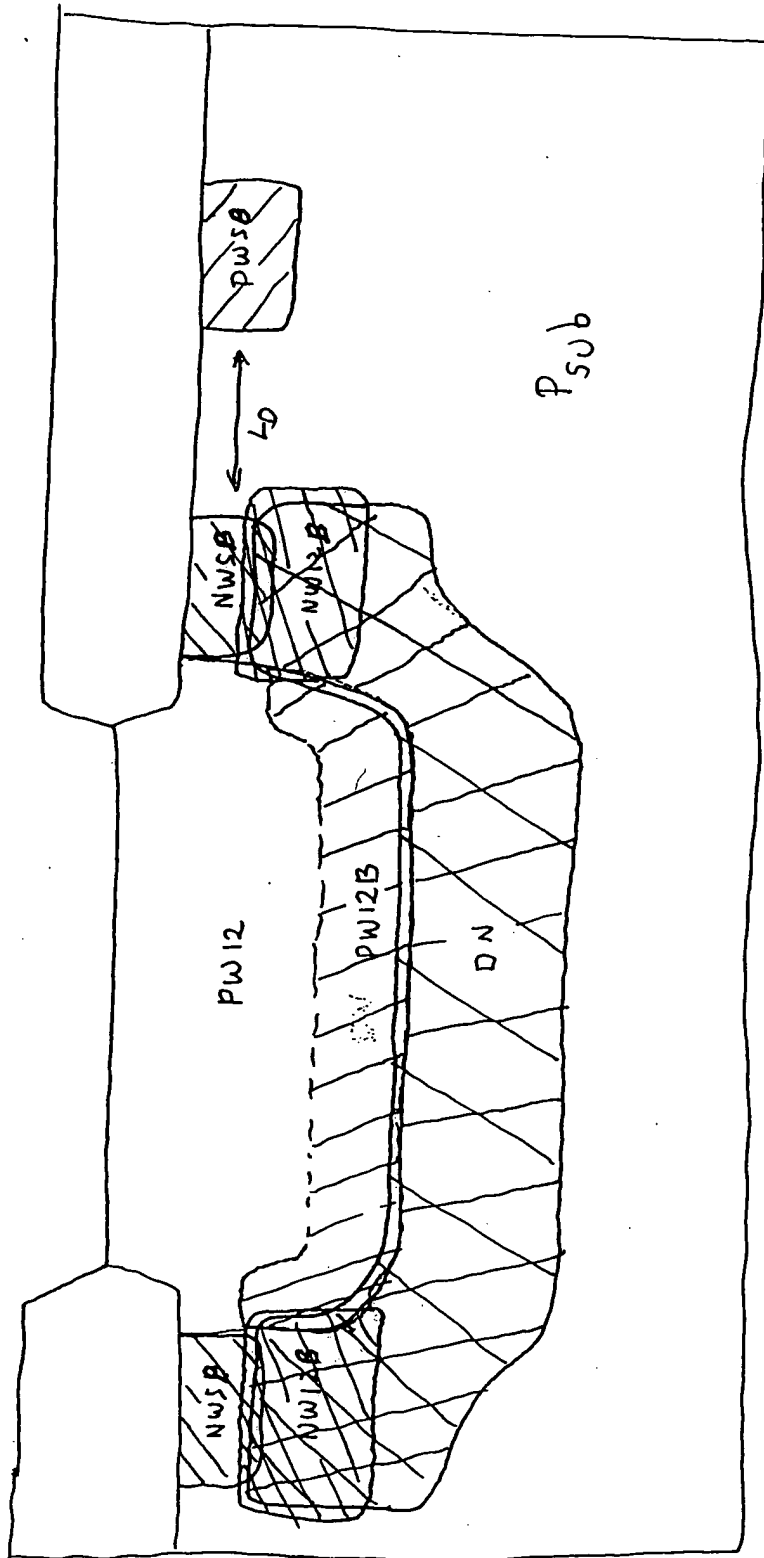


Fig. 15D

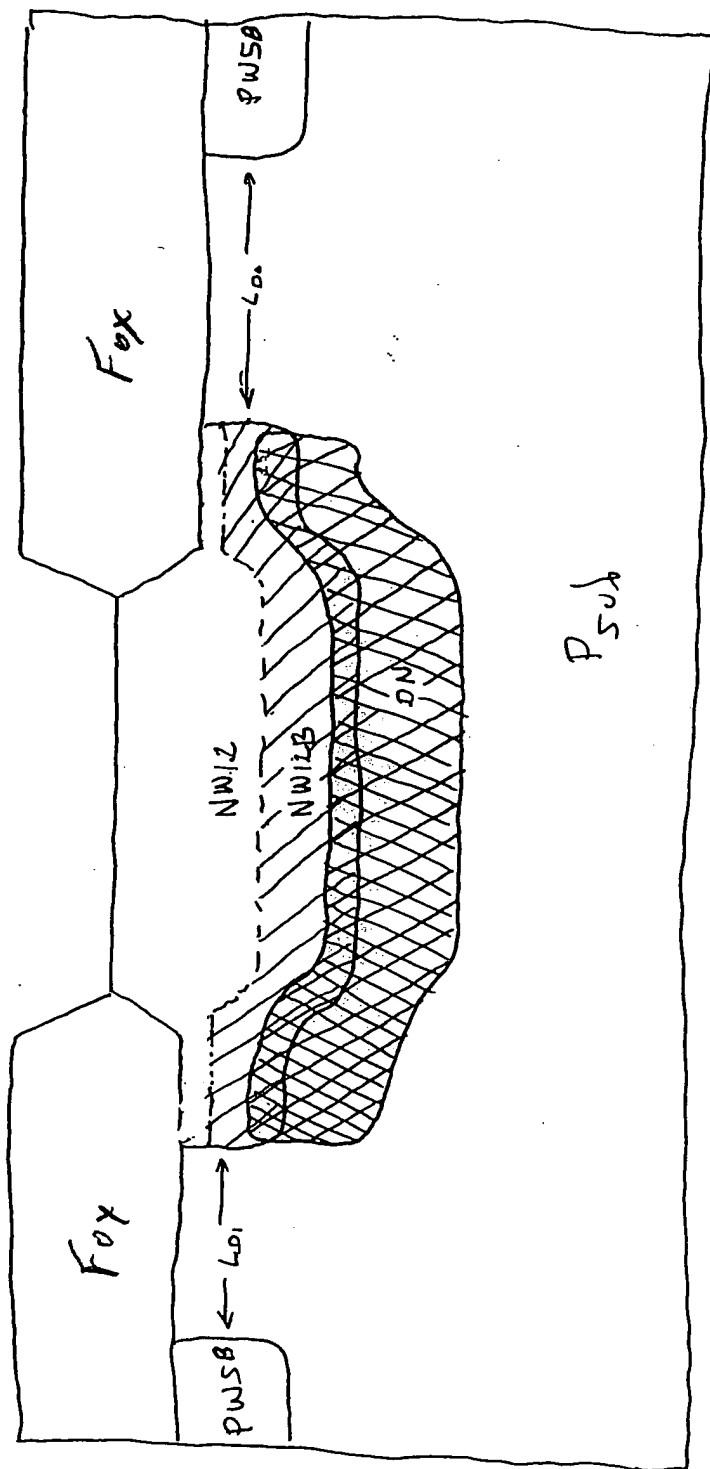


Fig. 15E

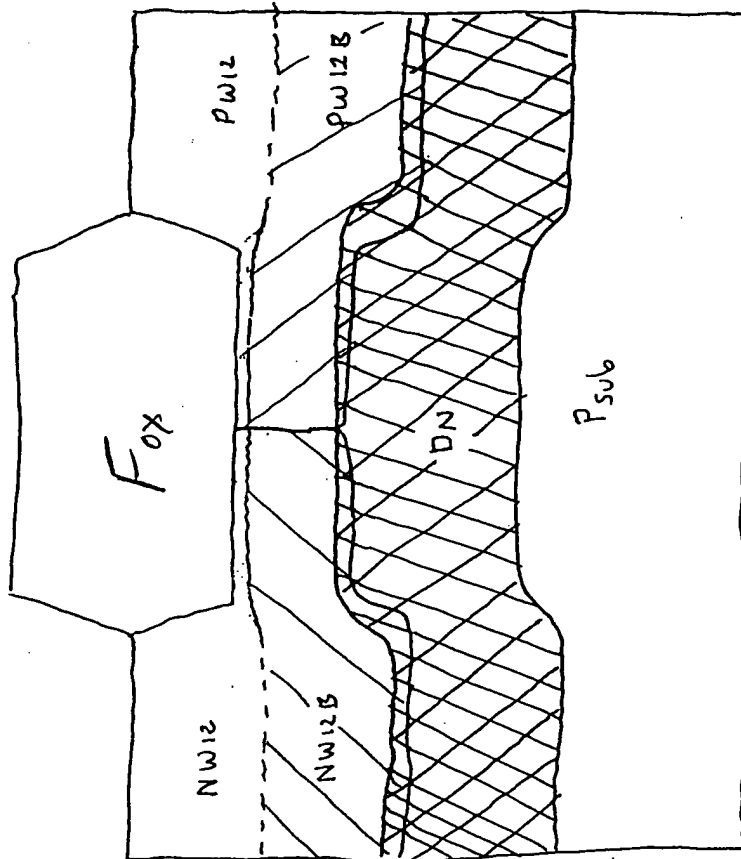


Fig. 15F

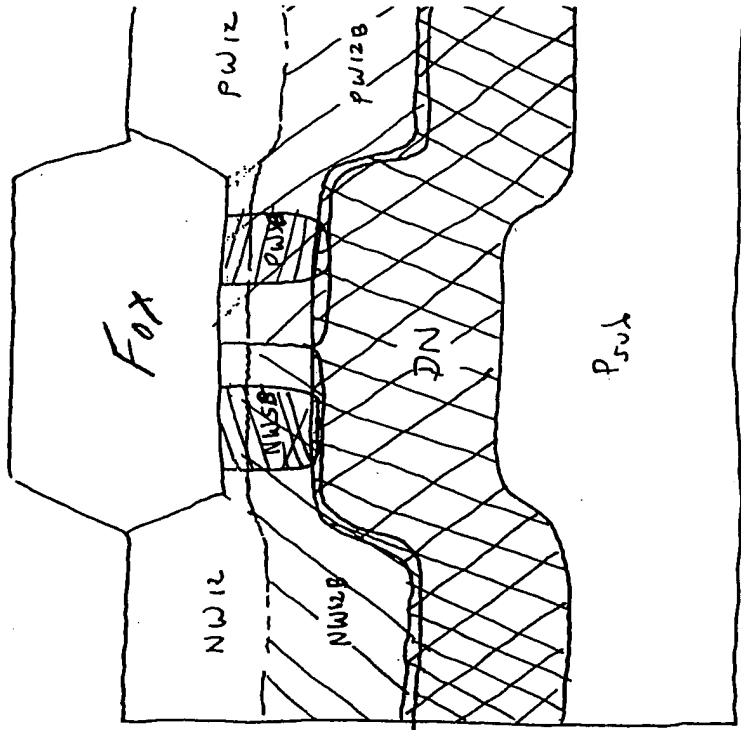
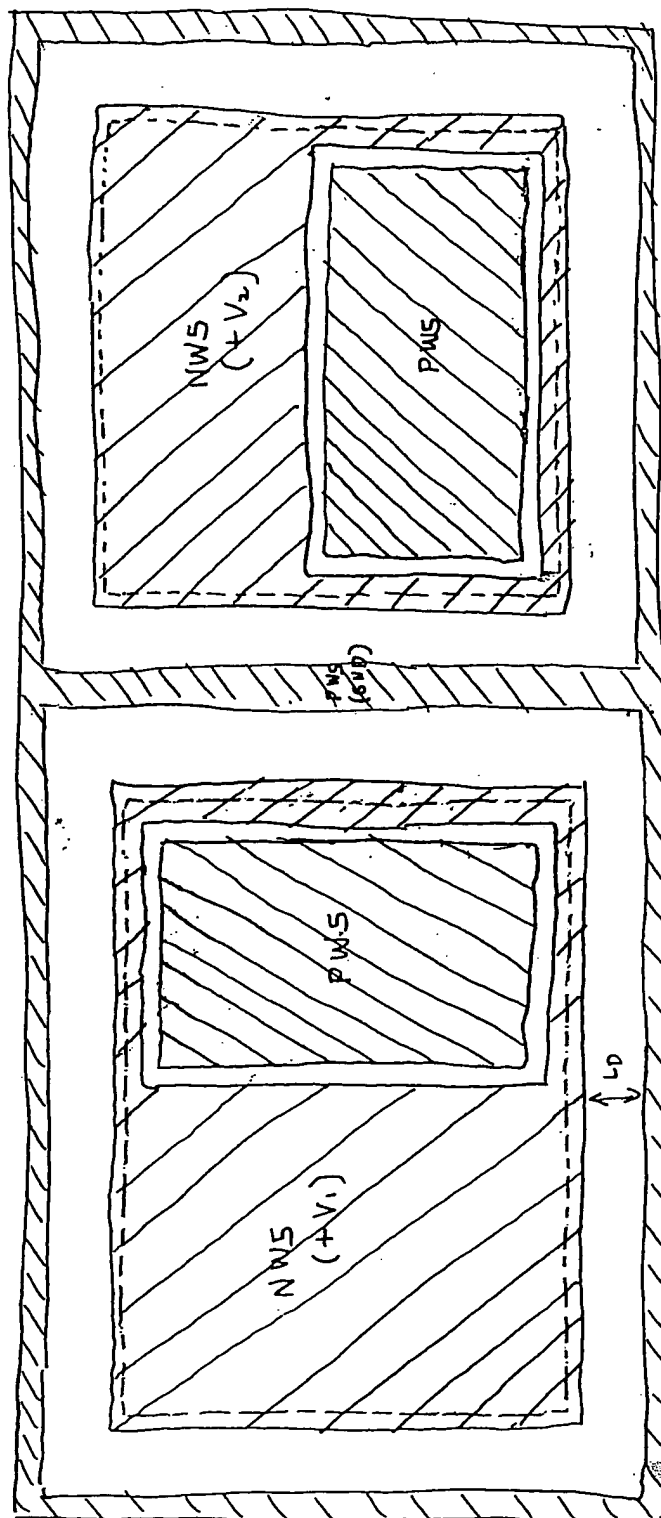
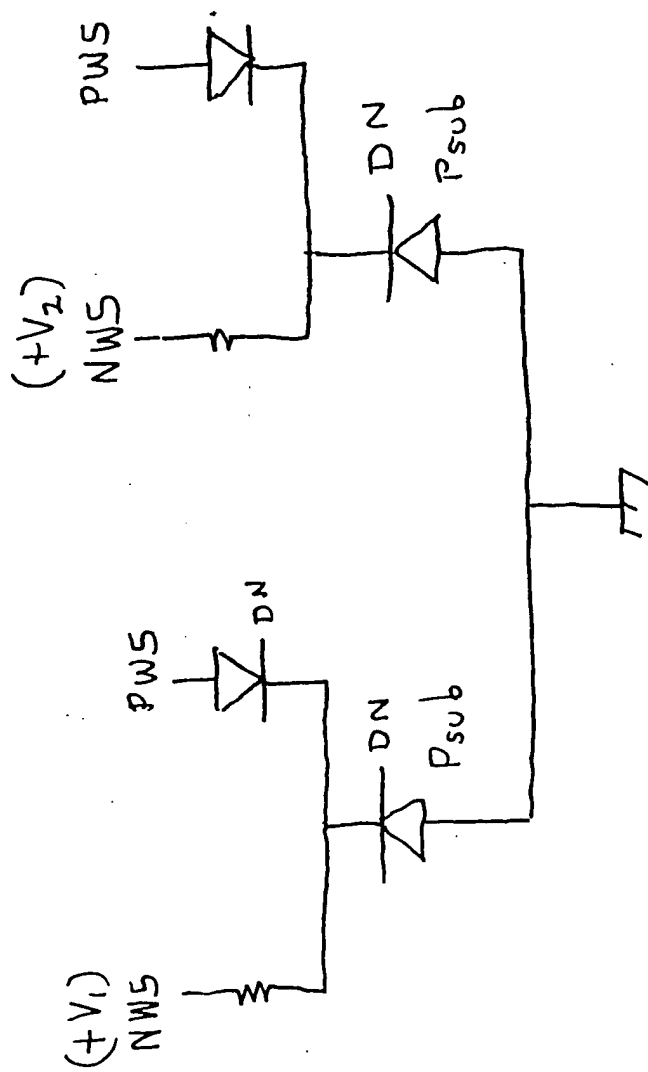


Fig. 16B



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Fig. 16C



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Fig. 16D

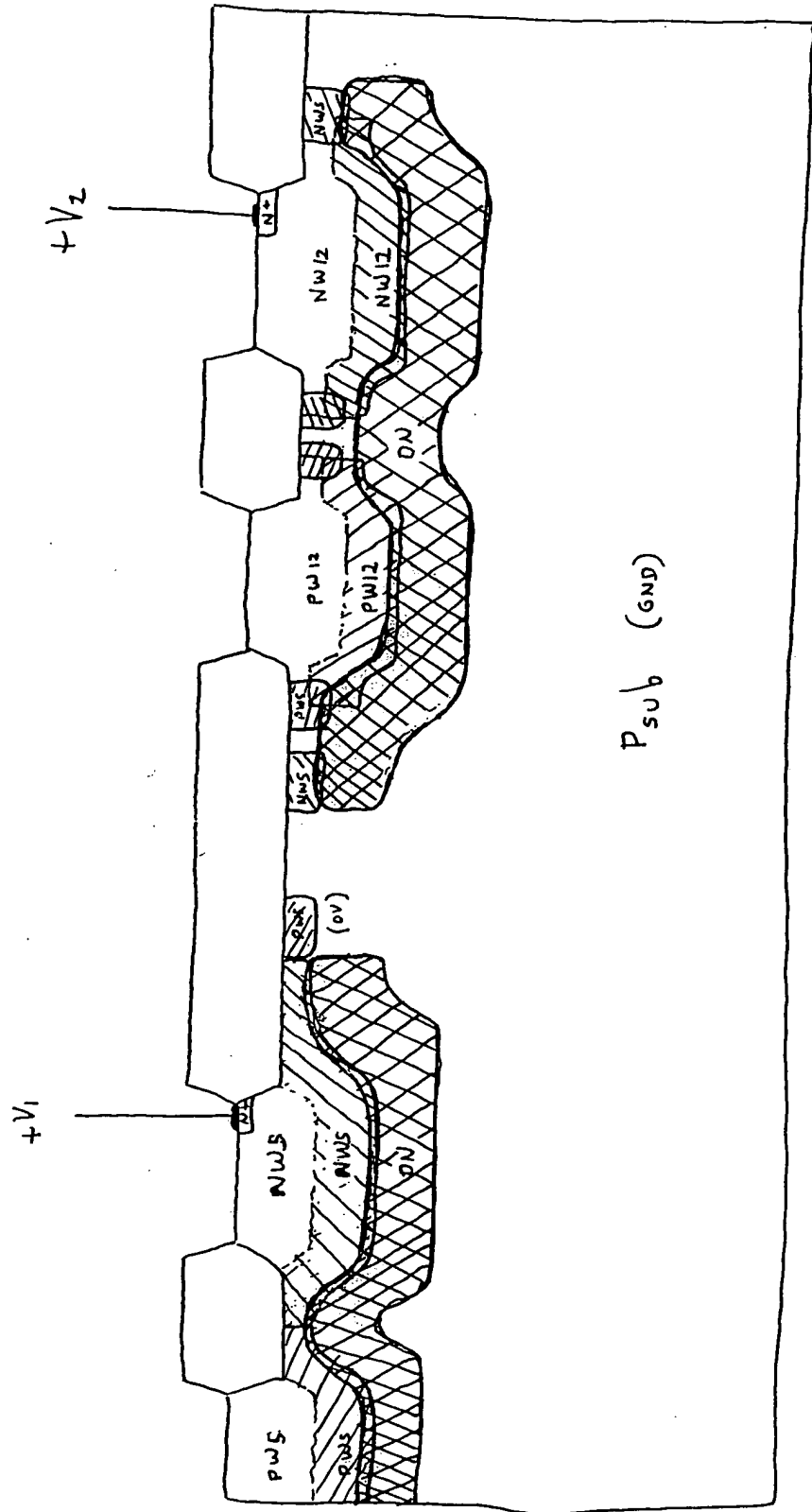
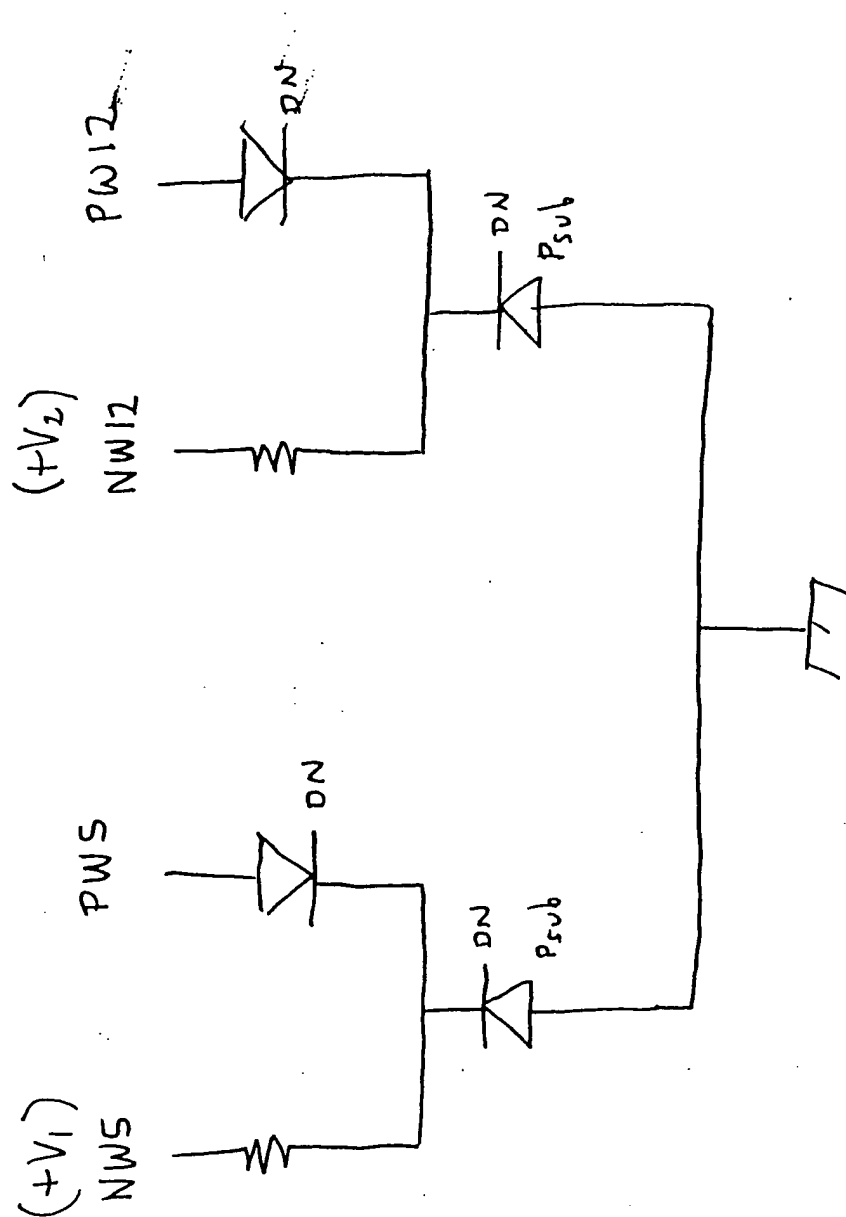


Fig. 16E



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Fig. 16F

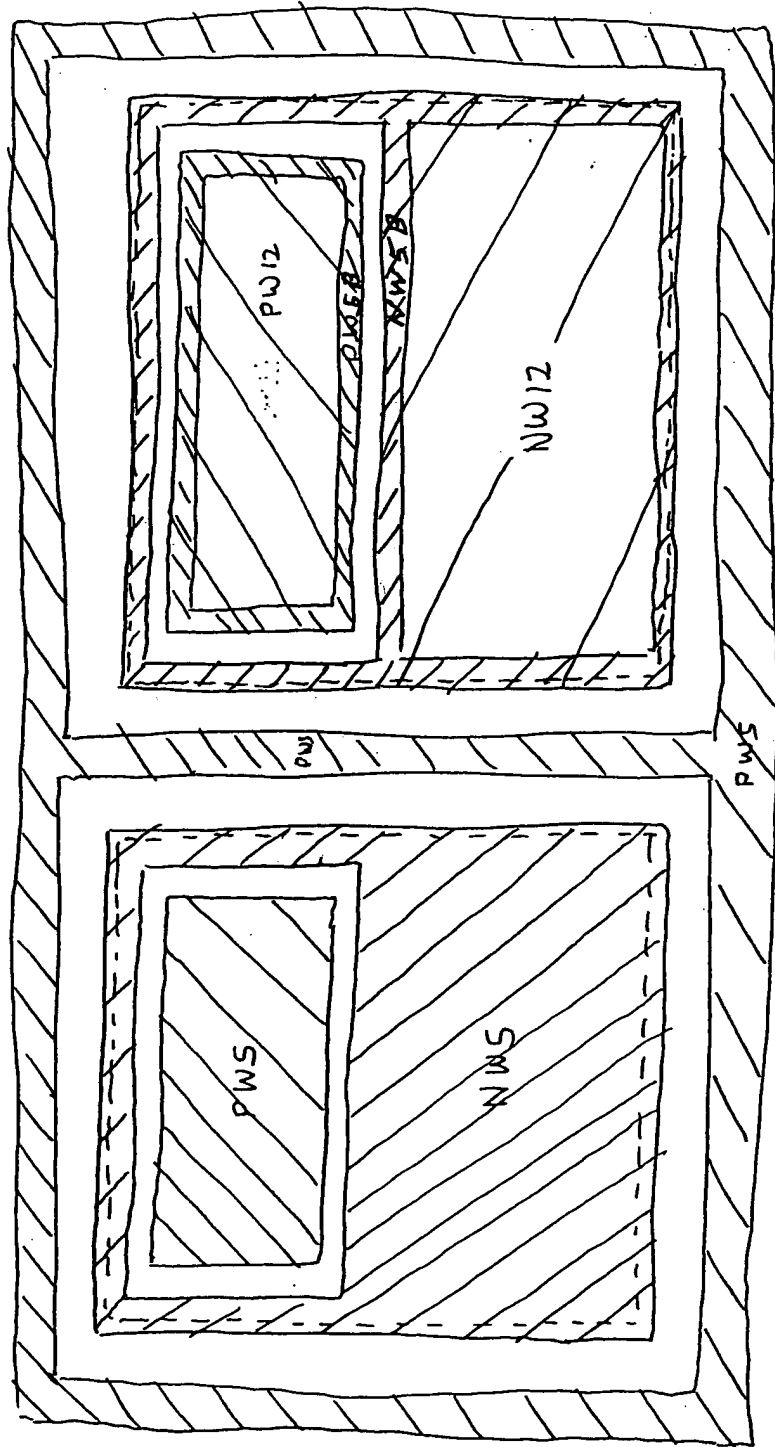


Fig. 17A

Prior Art

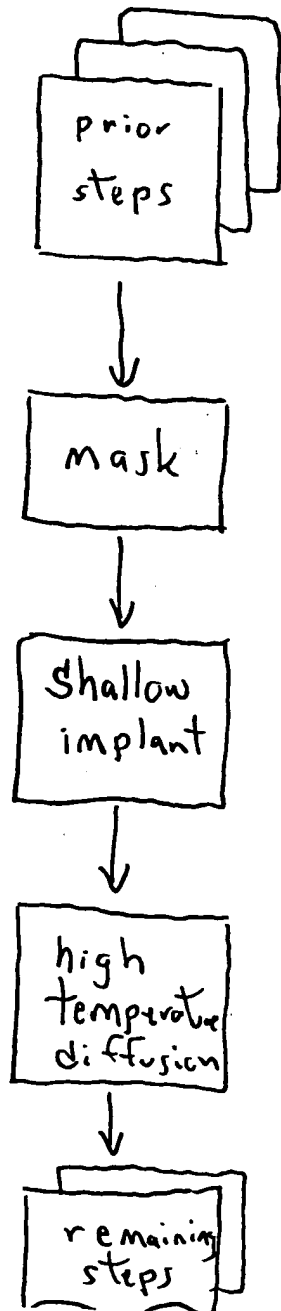


Fig. 17B

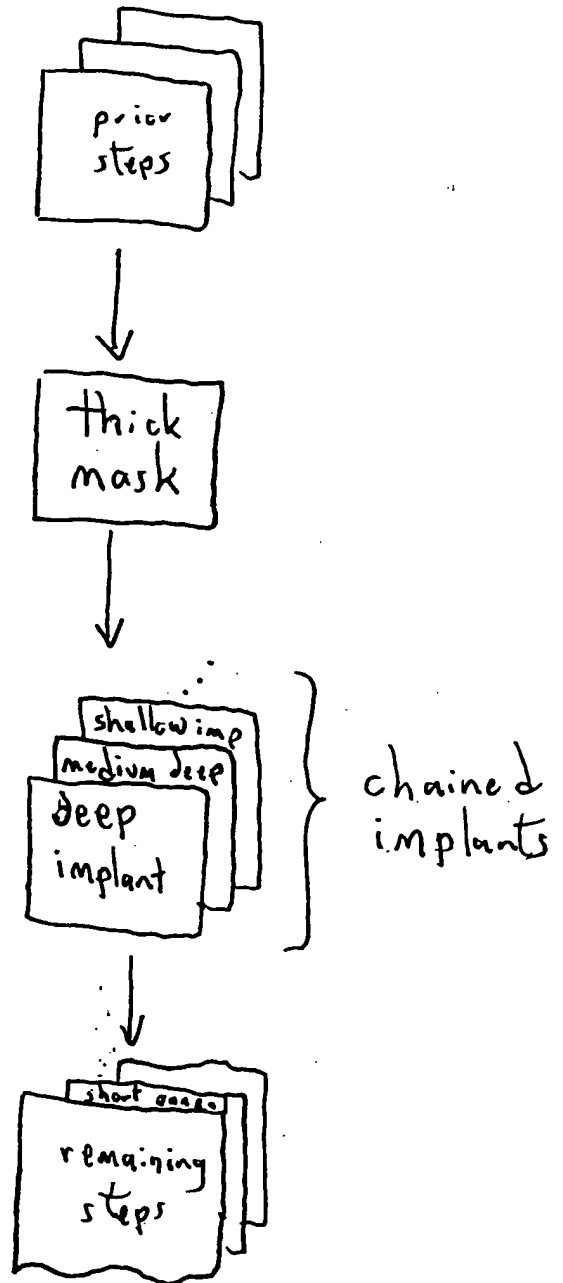


Fig. 17C

Prior Art

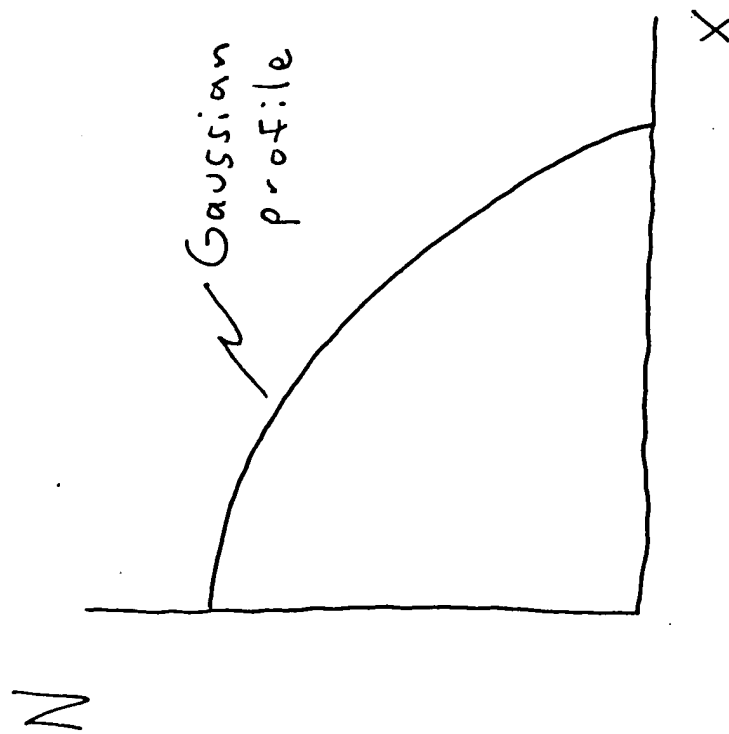


Fig. 17D

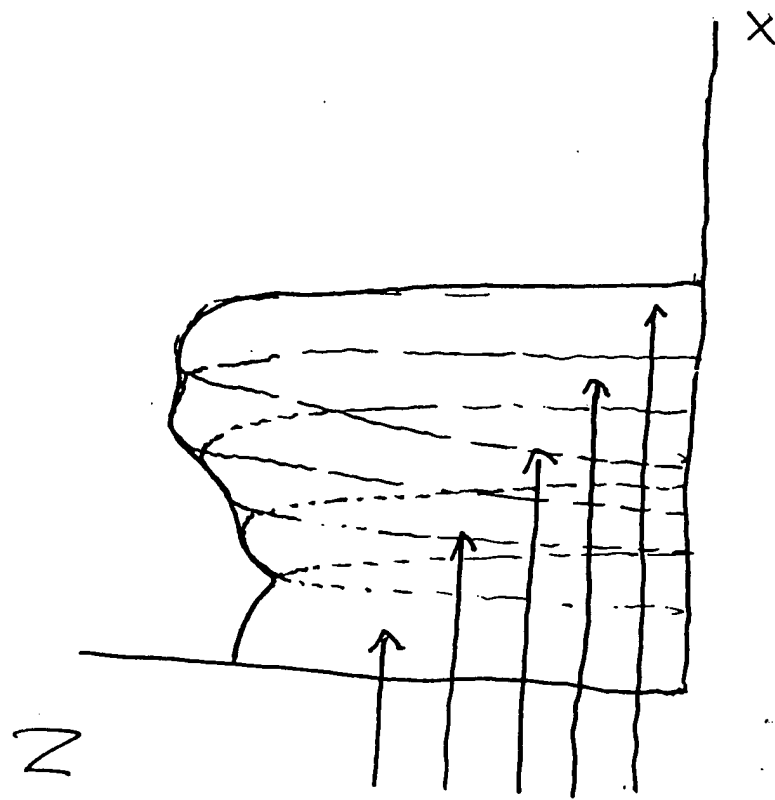


Fig. 17E

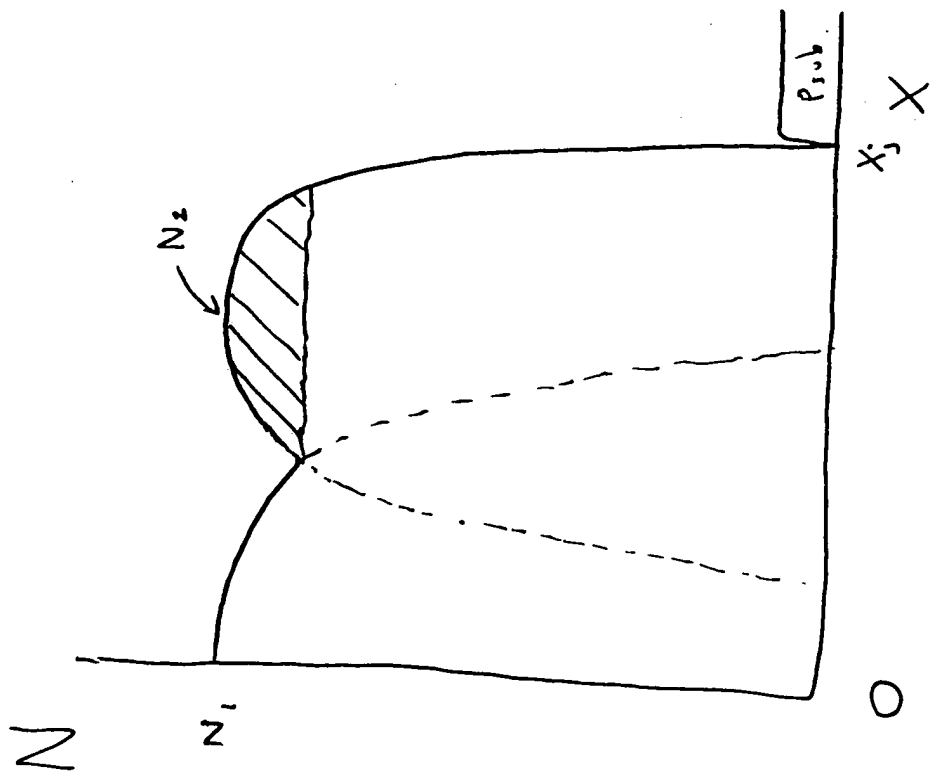


Fig. 17F

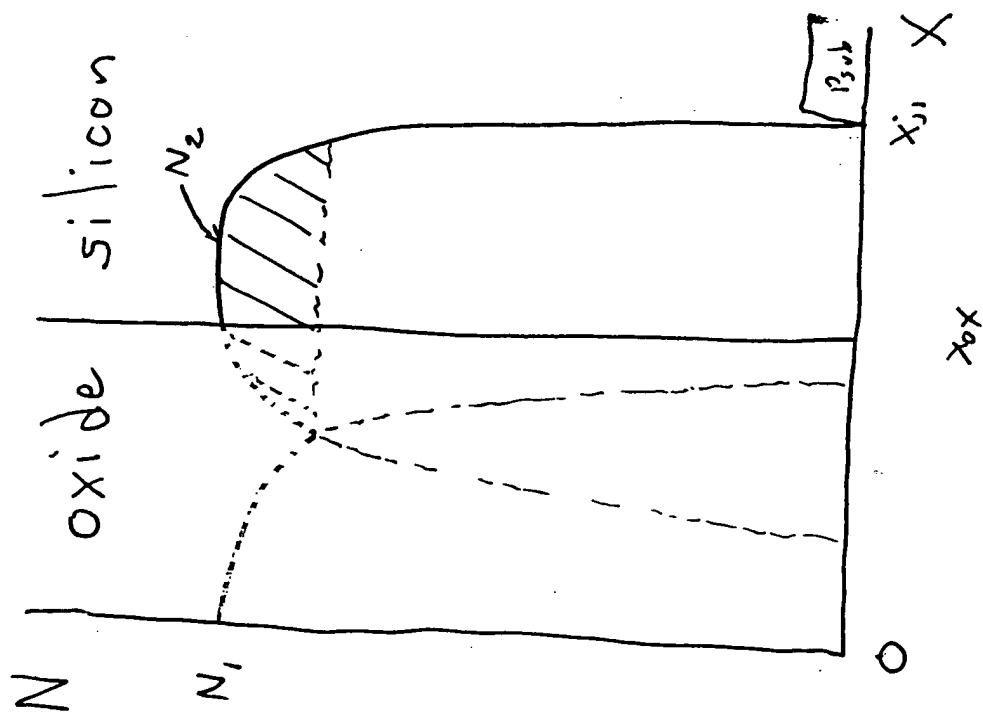


Fig. 176

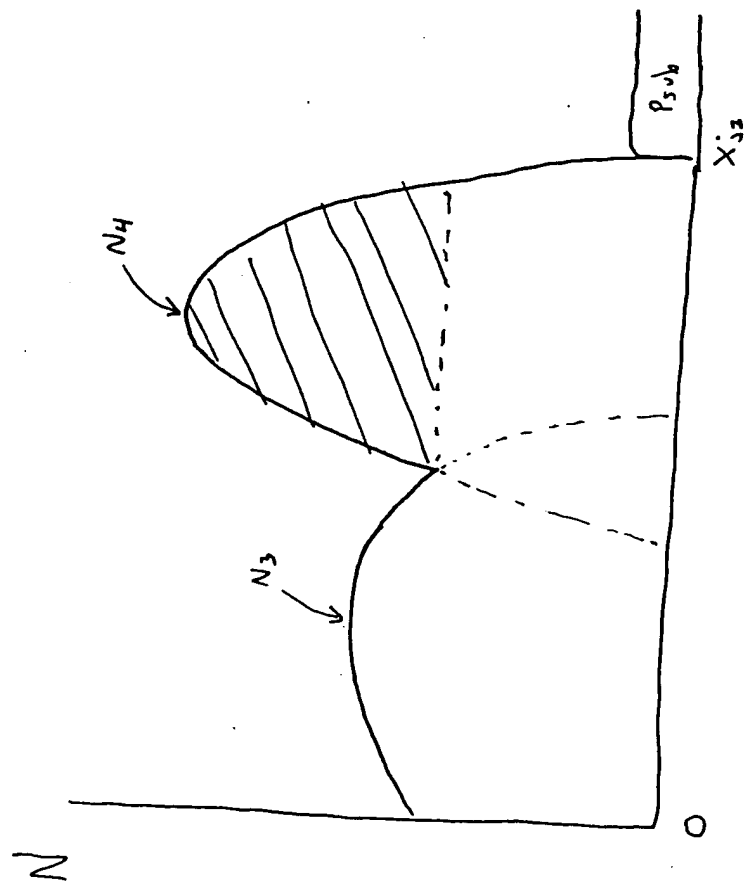


Fig. 17H

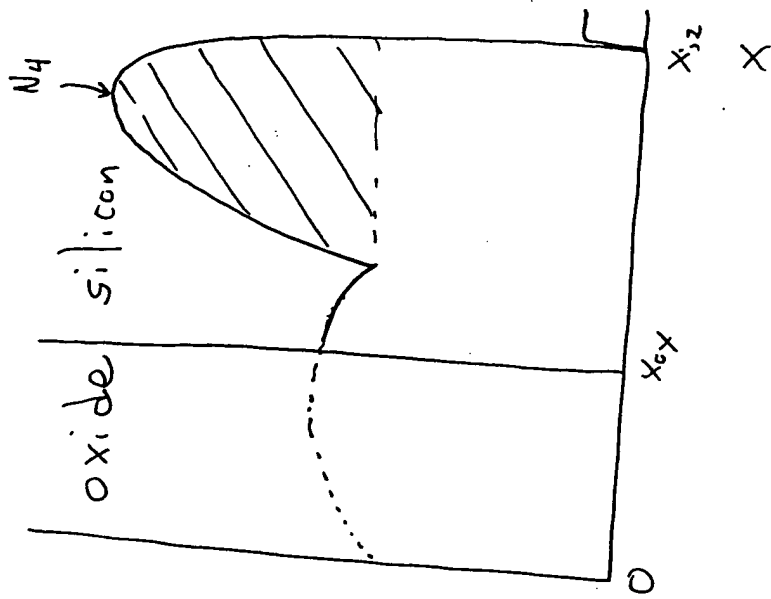


Fig. 17I

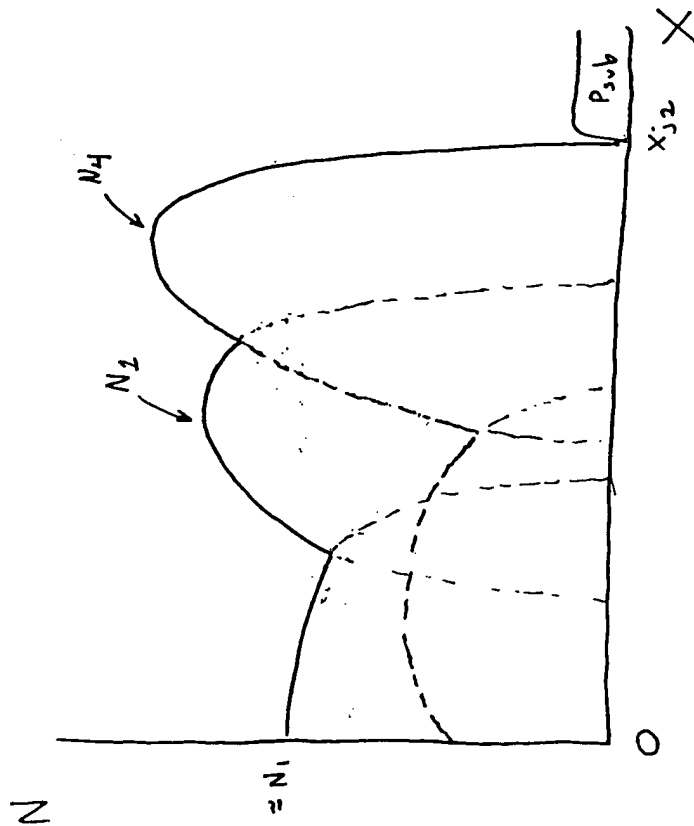
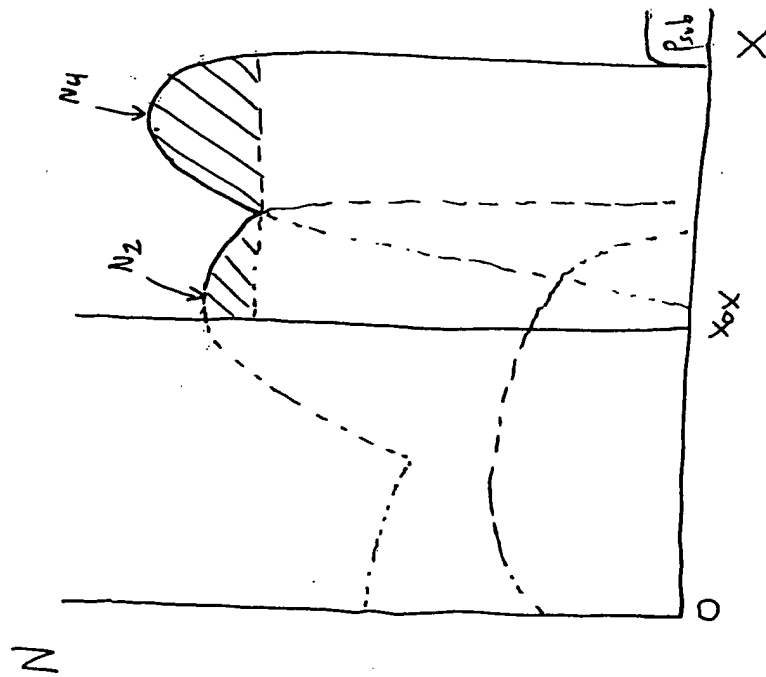


Fig. 17J



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Fig. 17K  
Prior Art

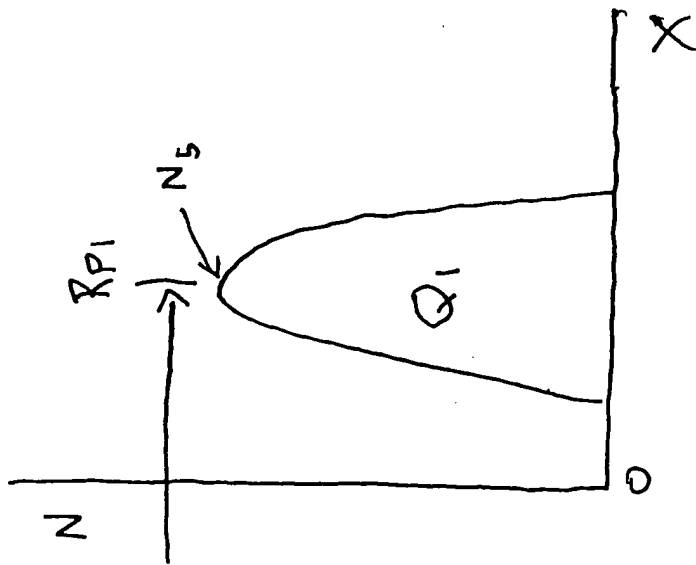


Fig. 17L  
Prior Art

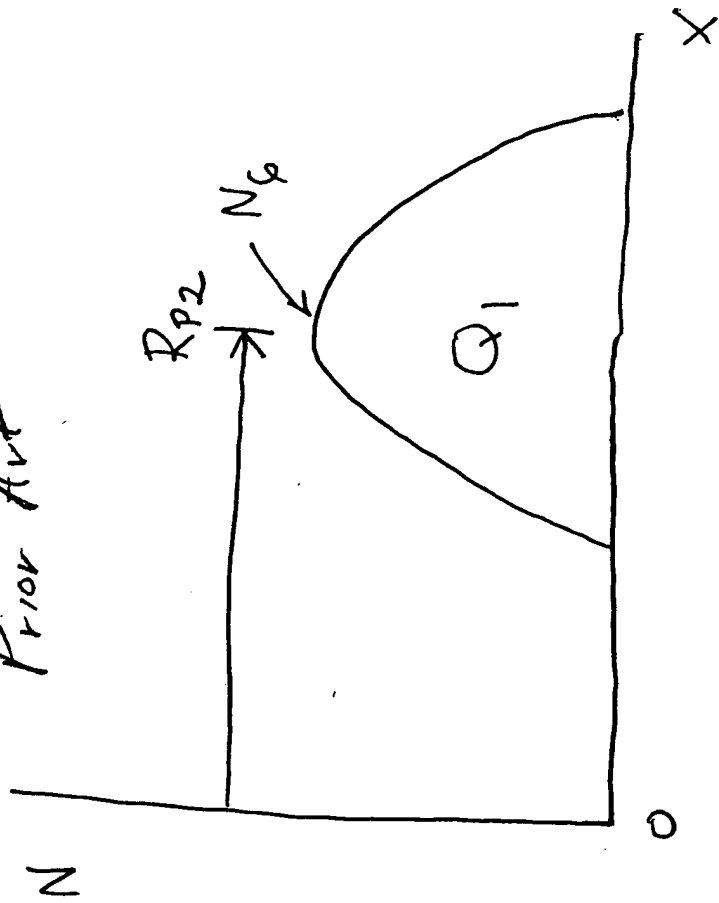


Fig. 17M

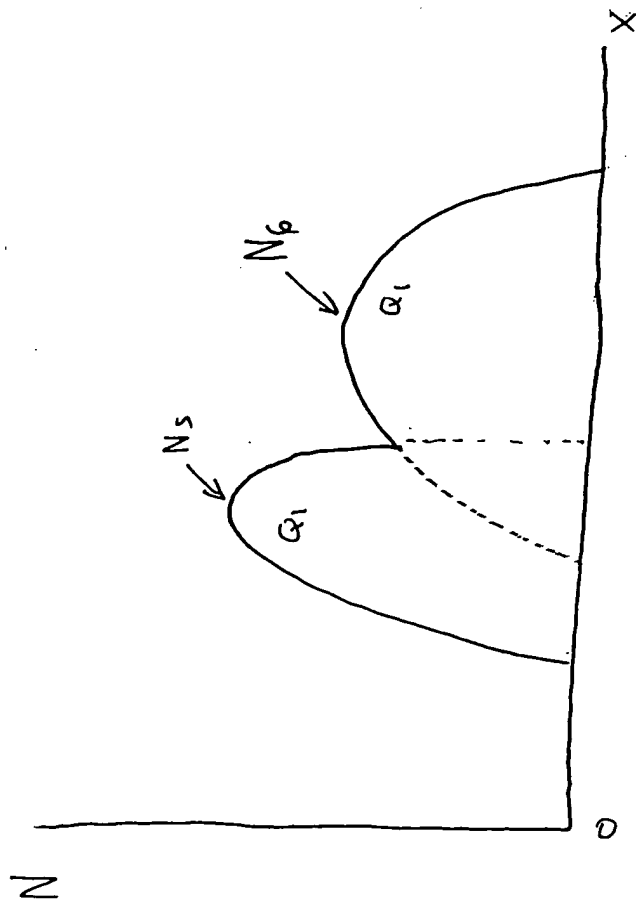


Fig. 17N

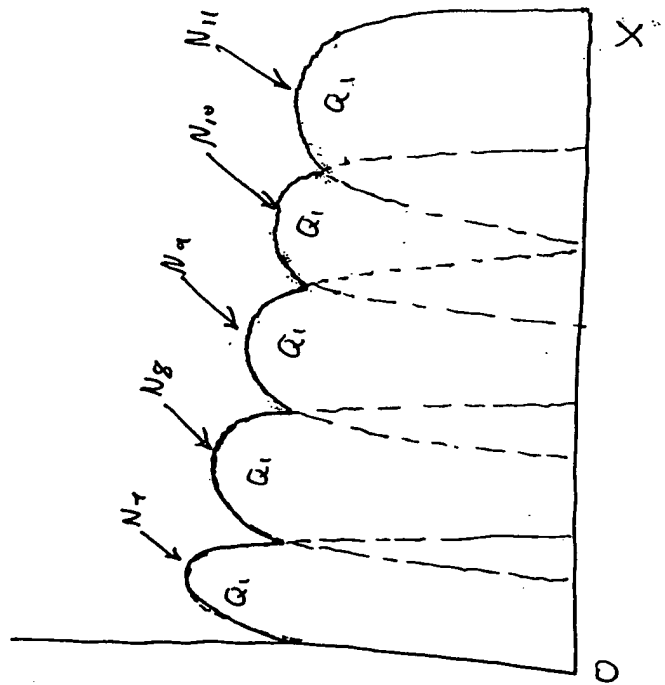




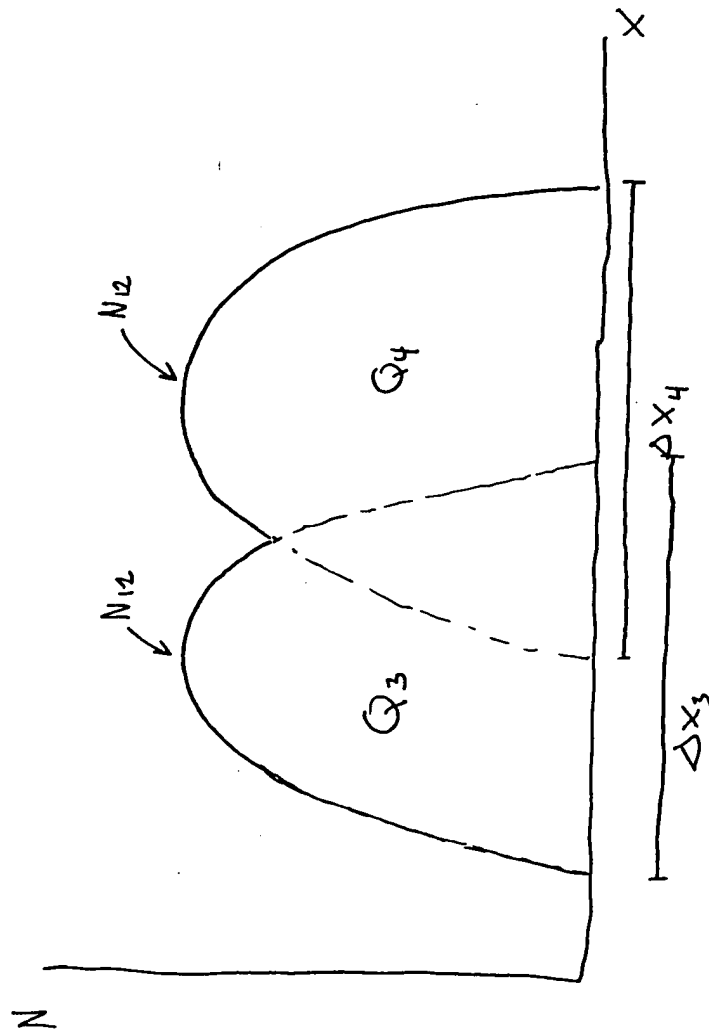
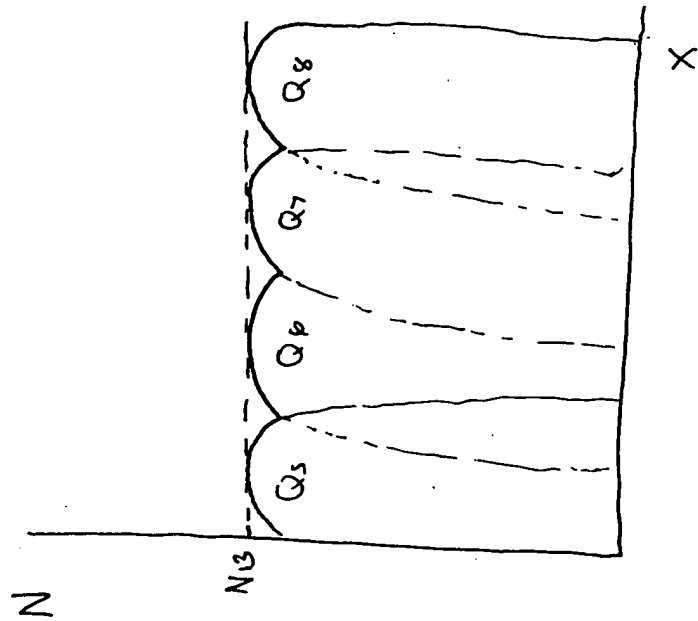
Fig. 17PFig. 17Q

Fig. 17R

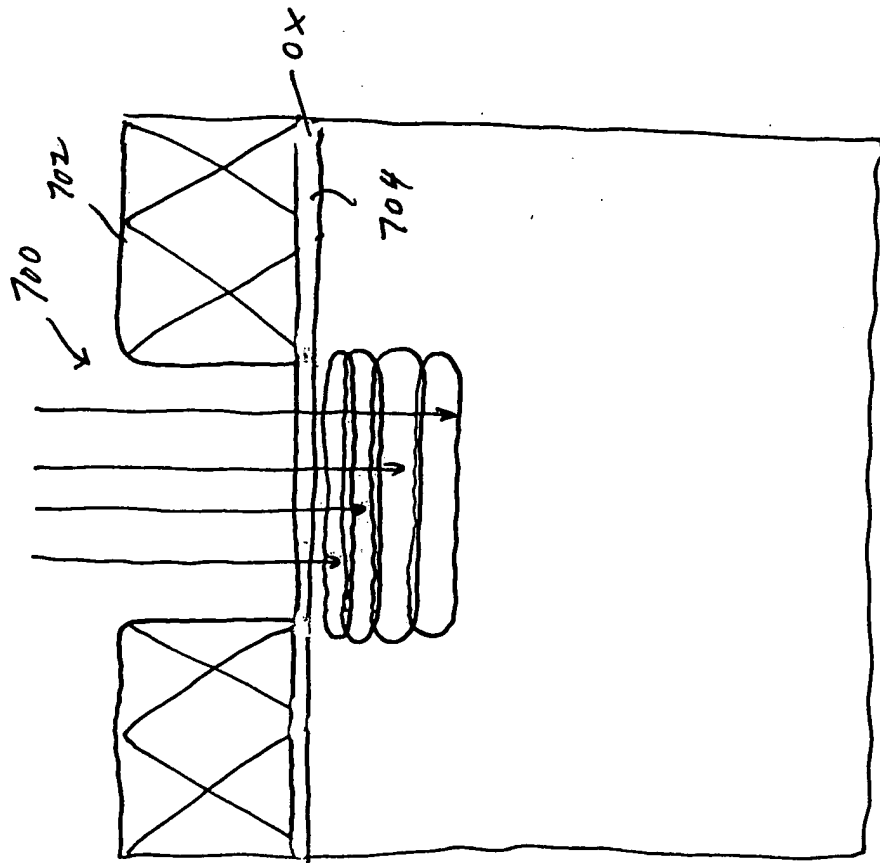
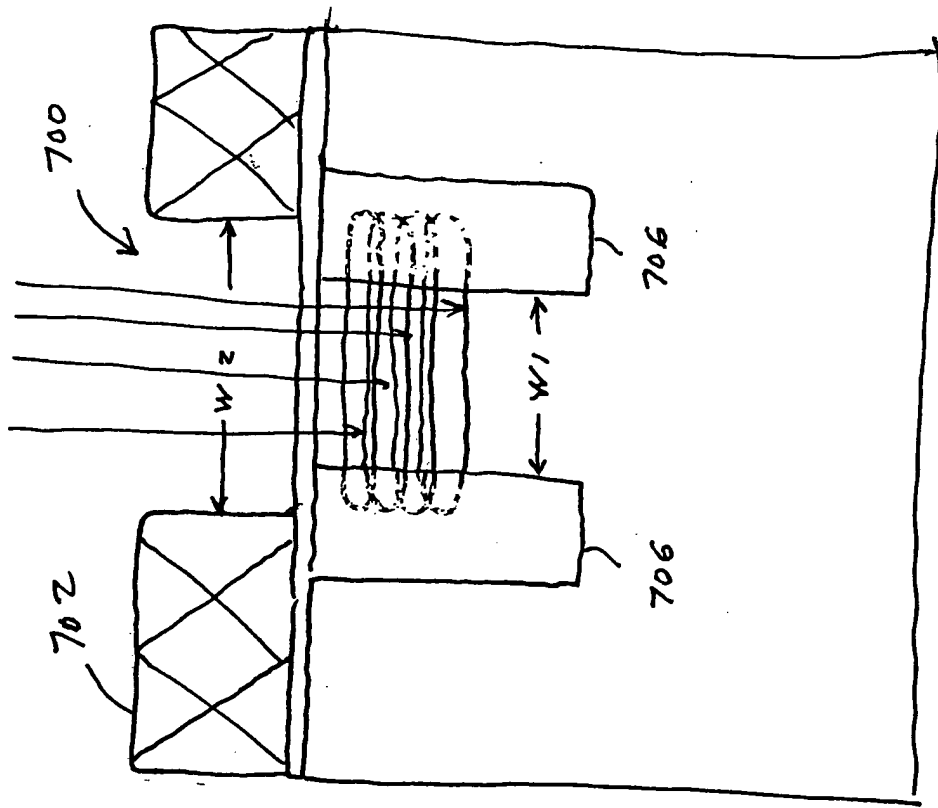


Fig. 17S



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Fig. 17T

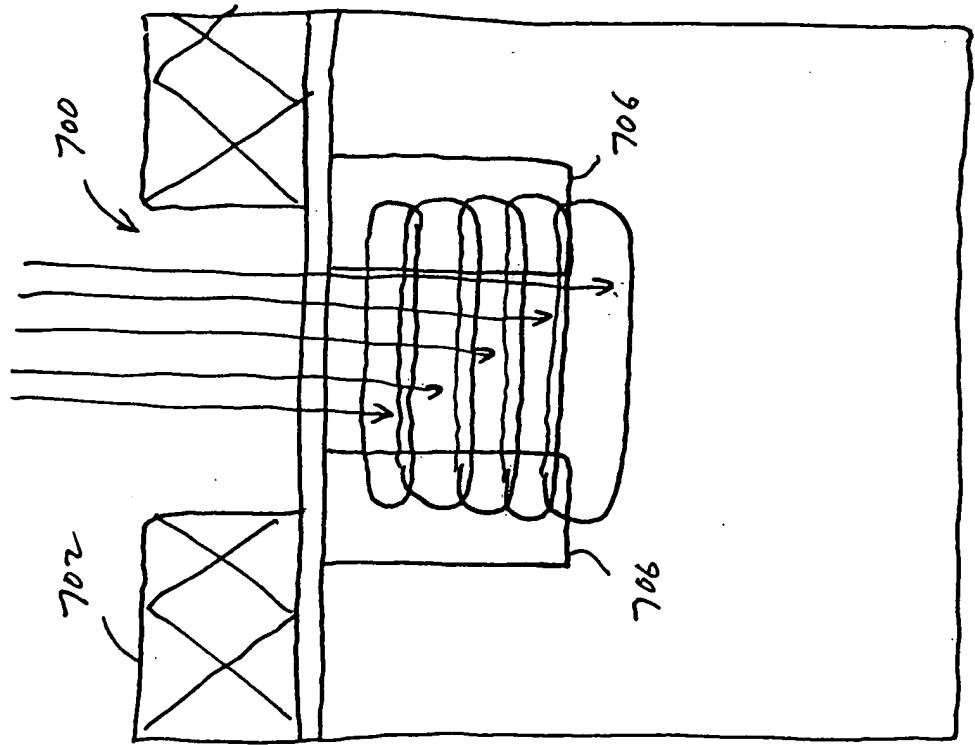
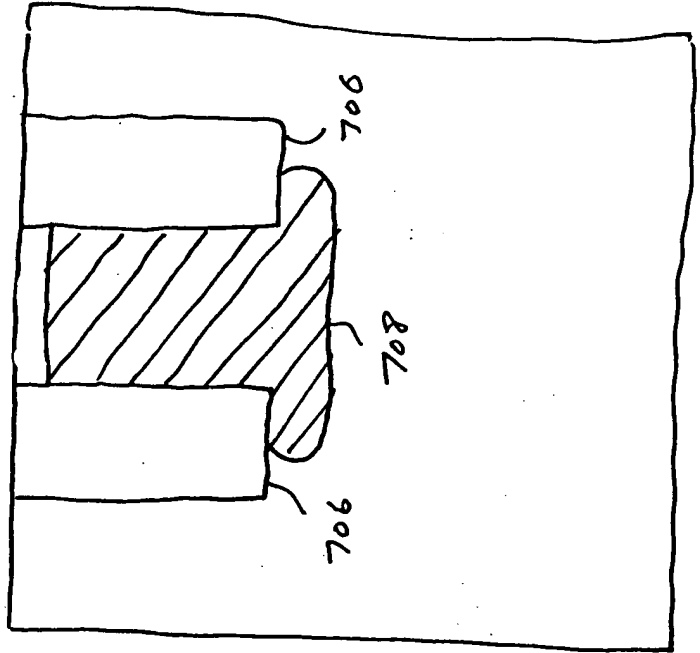


Fig. 17U



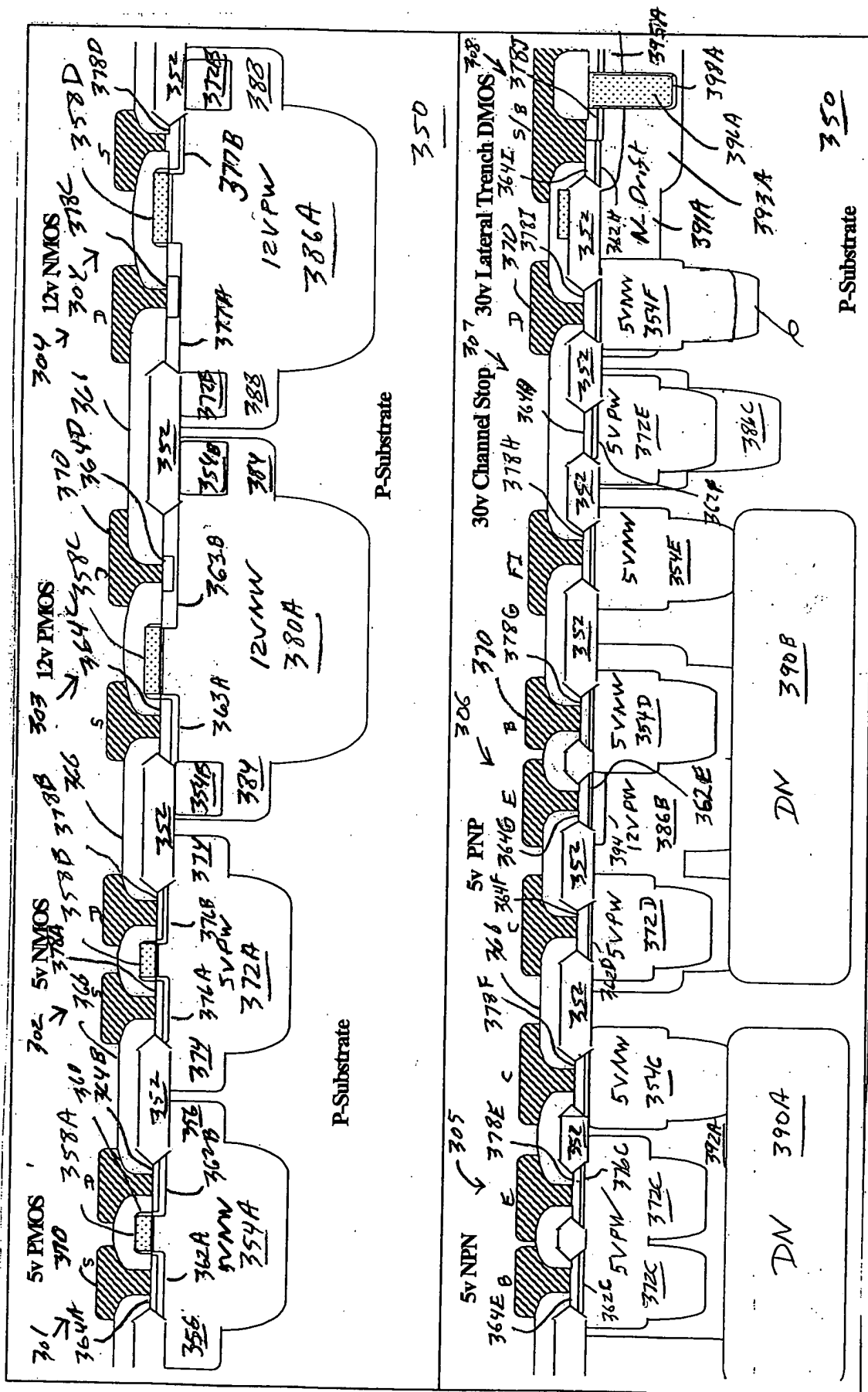


Fig. 18A

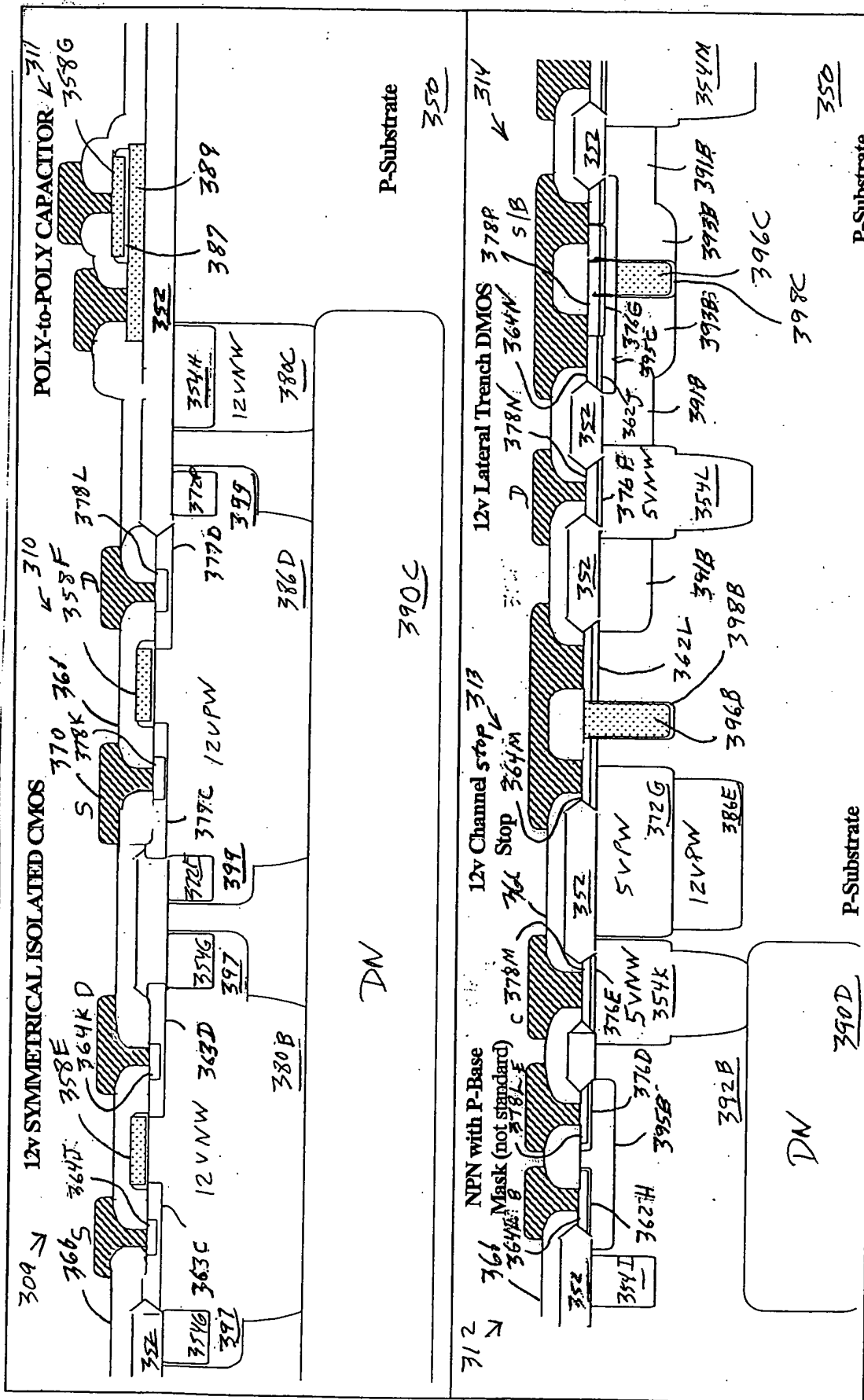
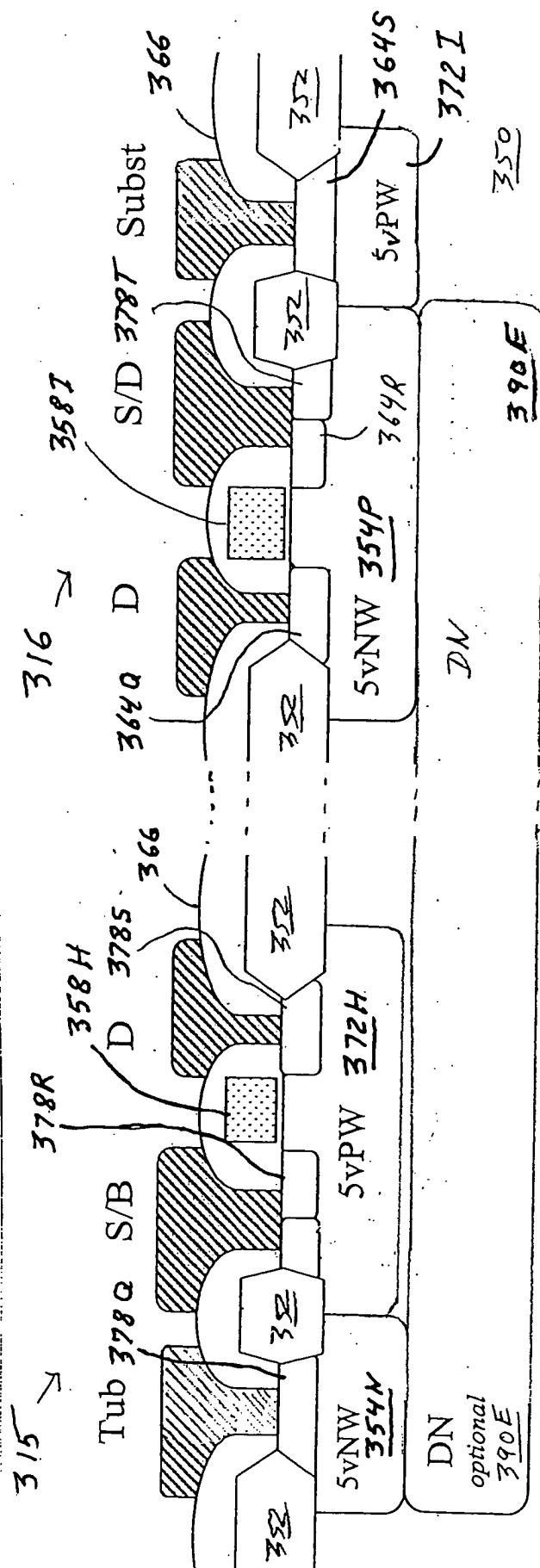


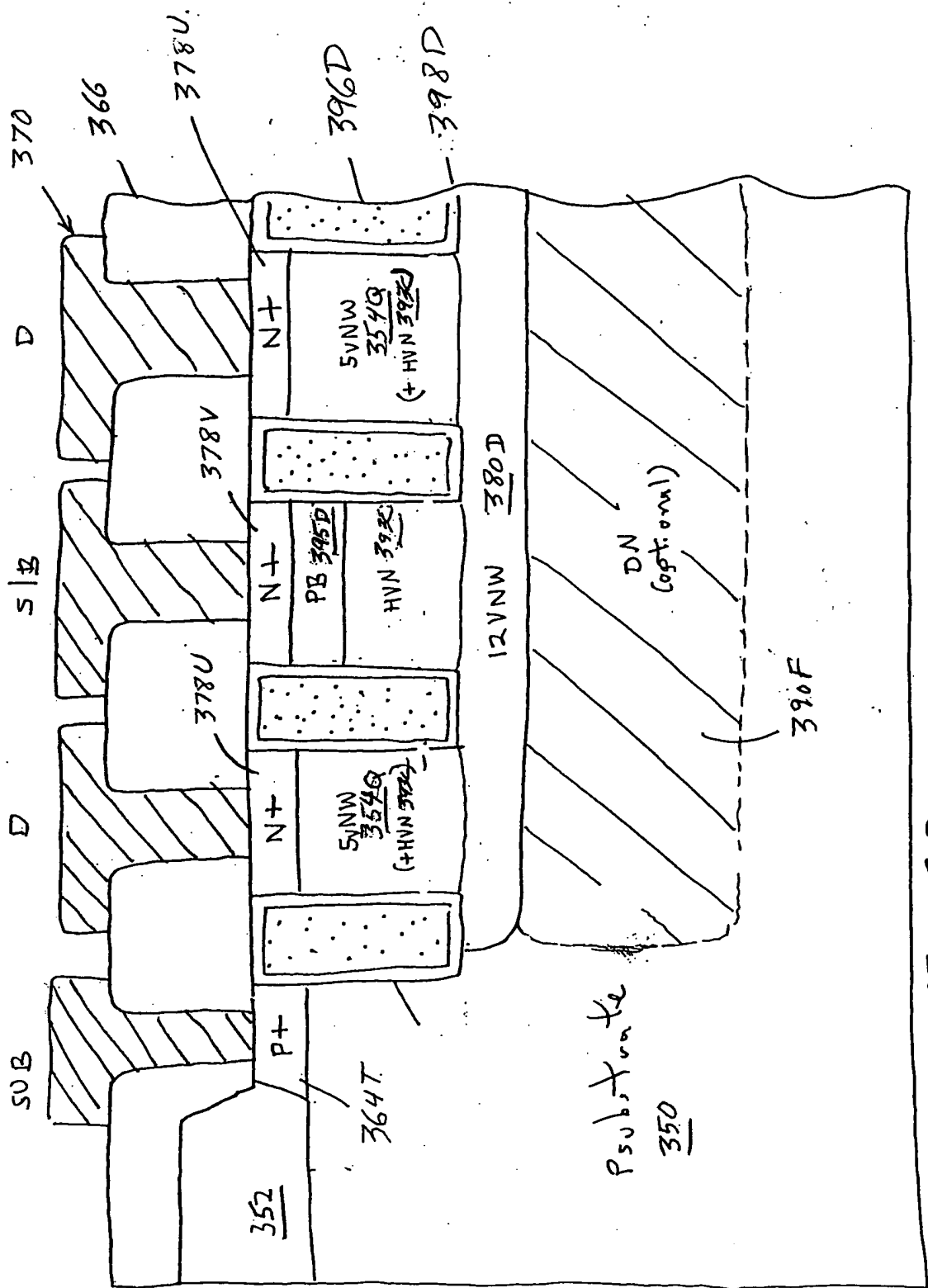
Fig. 18B



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300

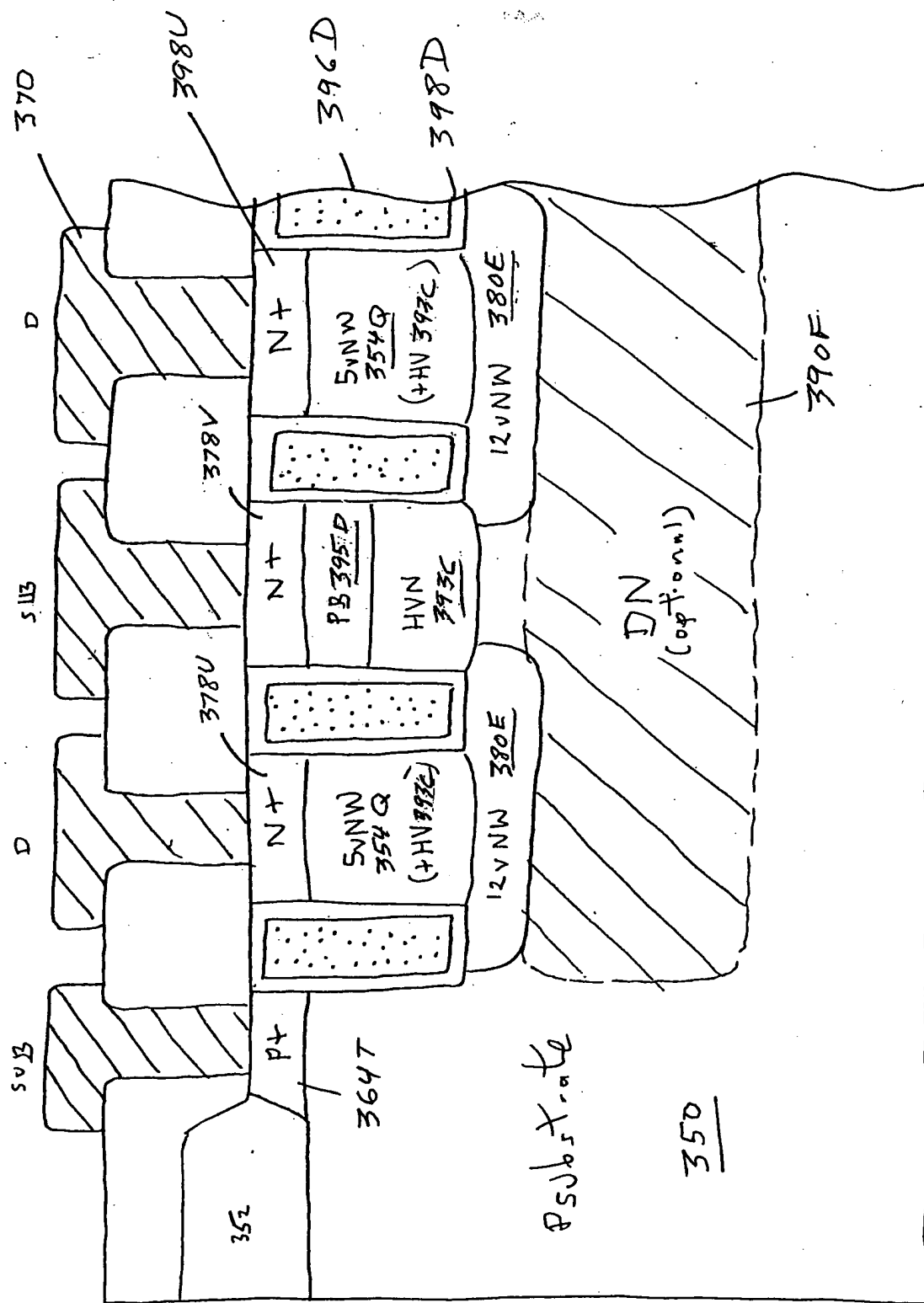
317



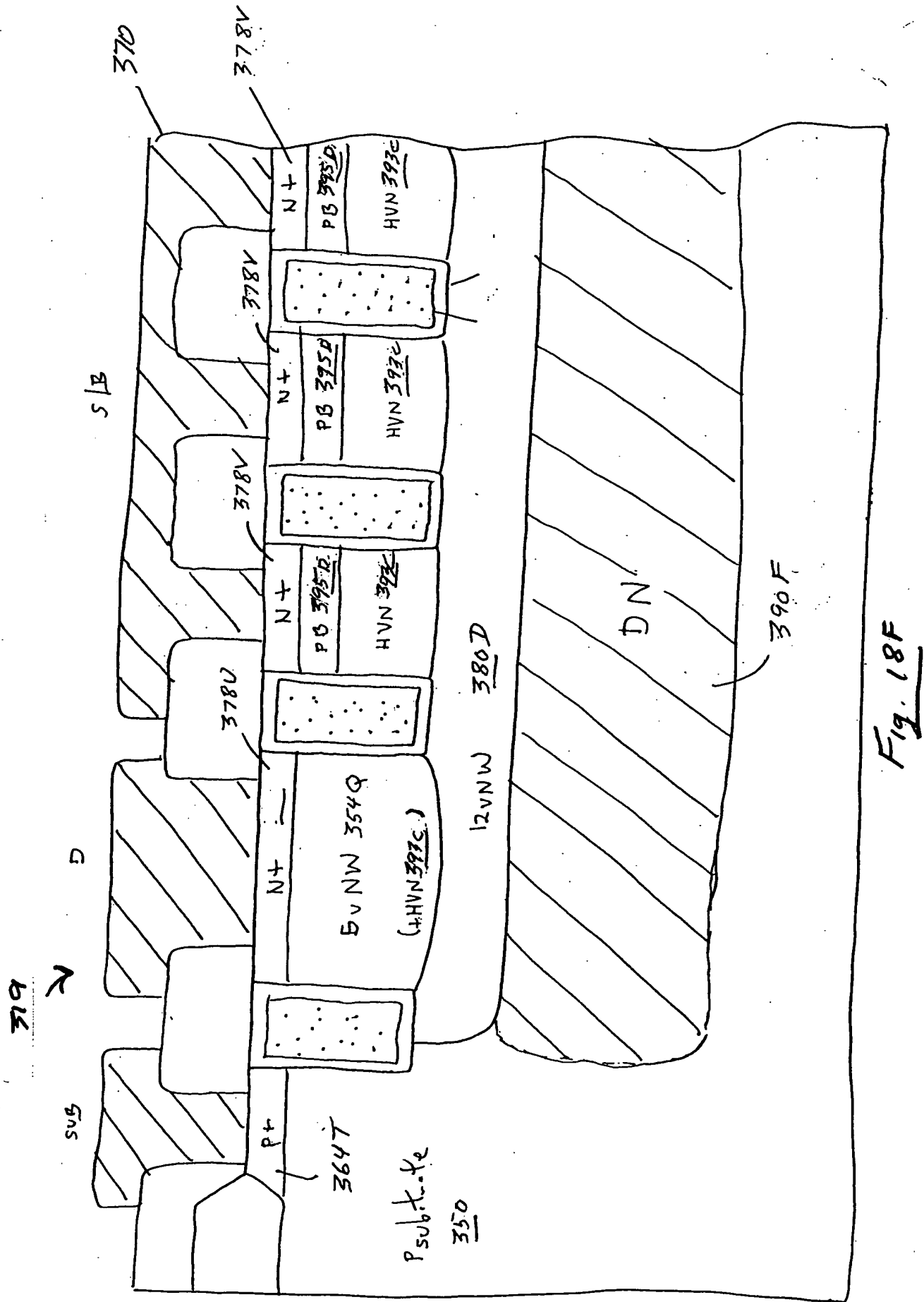
80/219

300

3/8







320  
↓

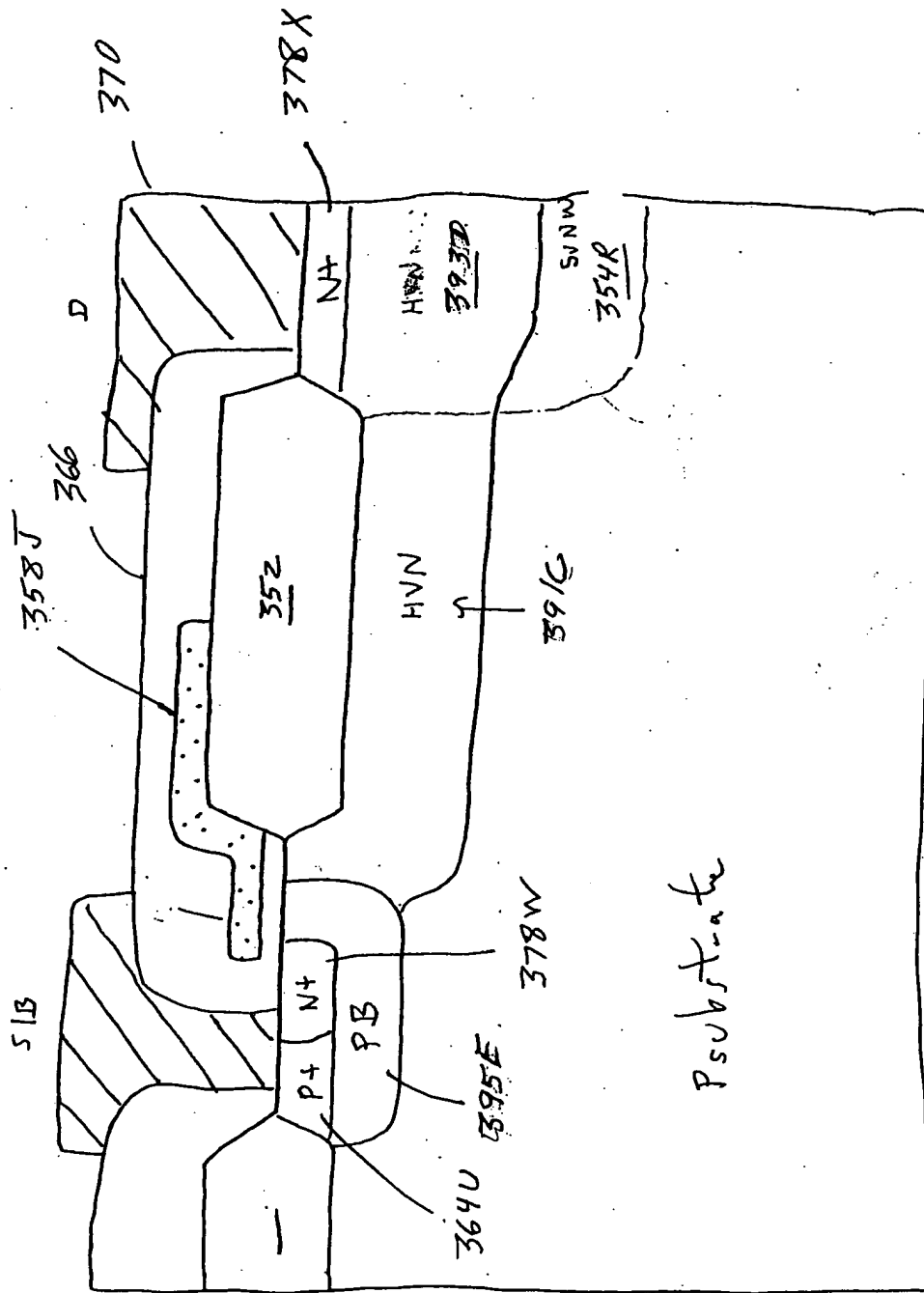
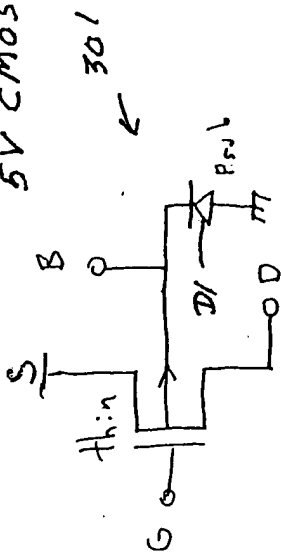
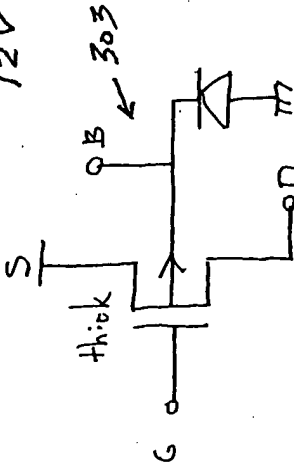


Fig 186

5V CMOS



12V CMOS



30V Trench LDMOS

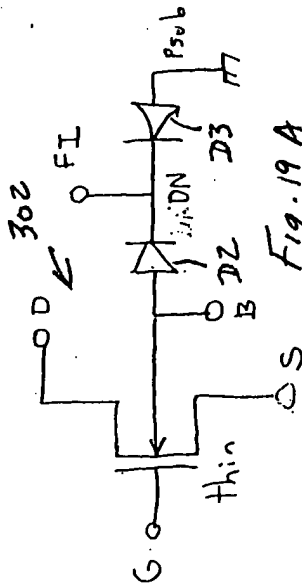
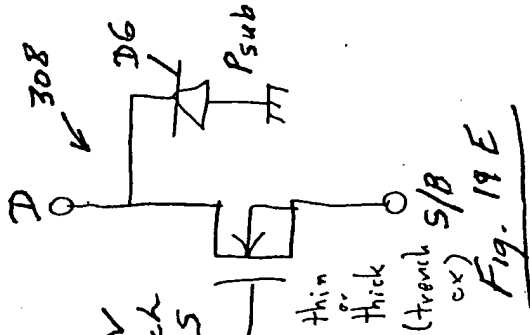


Fig. 19A

5V NPN

5V PNP

30V LDMOS

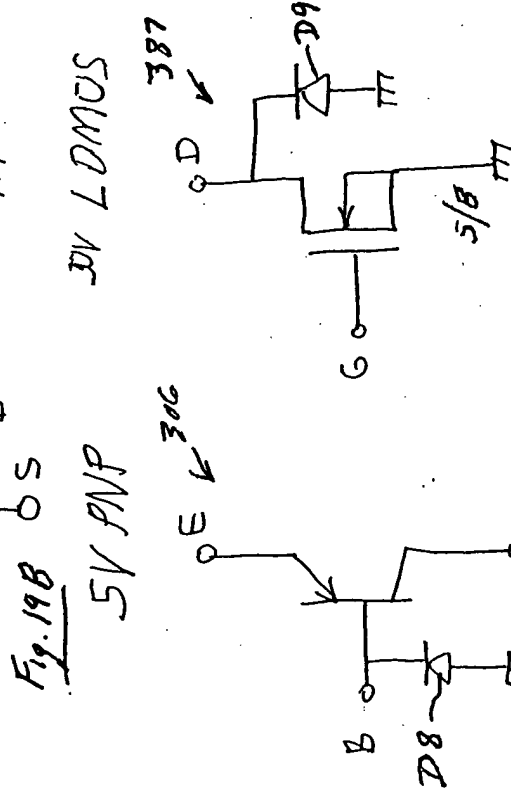


Fig. 19D

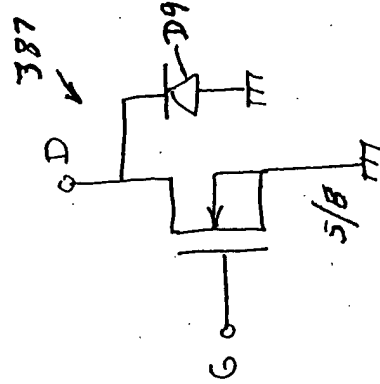


Fig. 19H

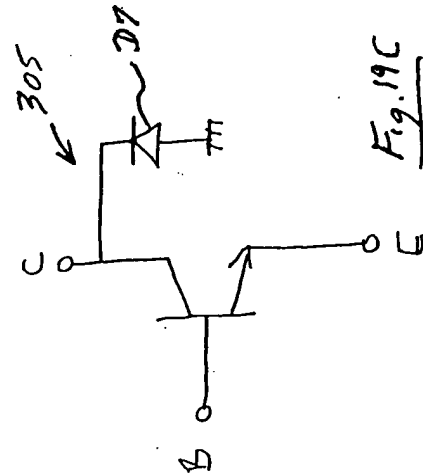


Fig. 19C

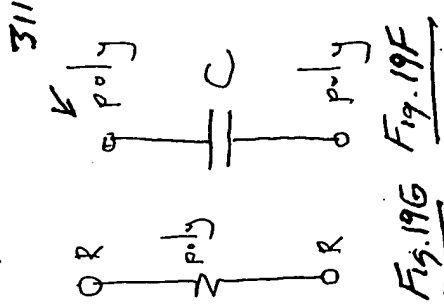


Fig. 19E

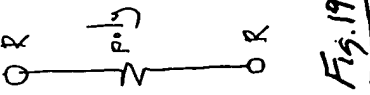


Fig. 19G

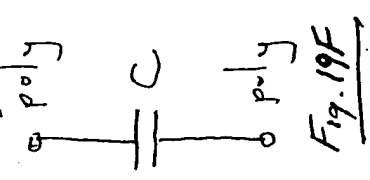
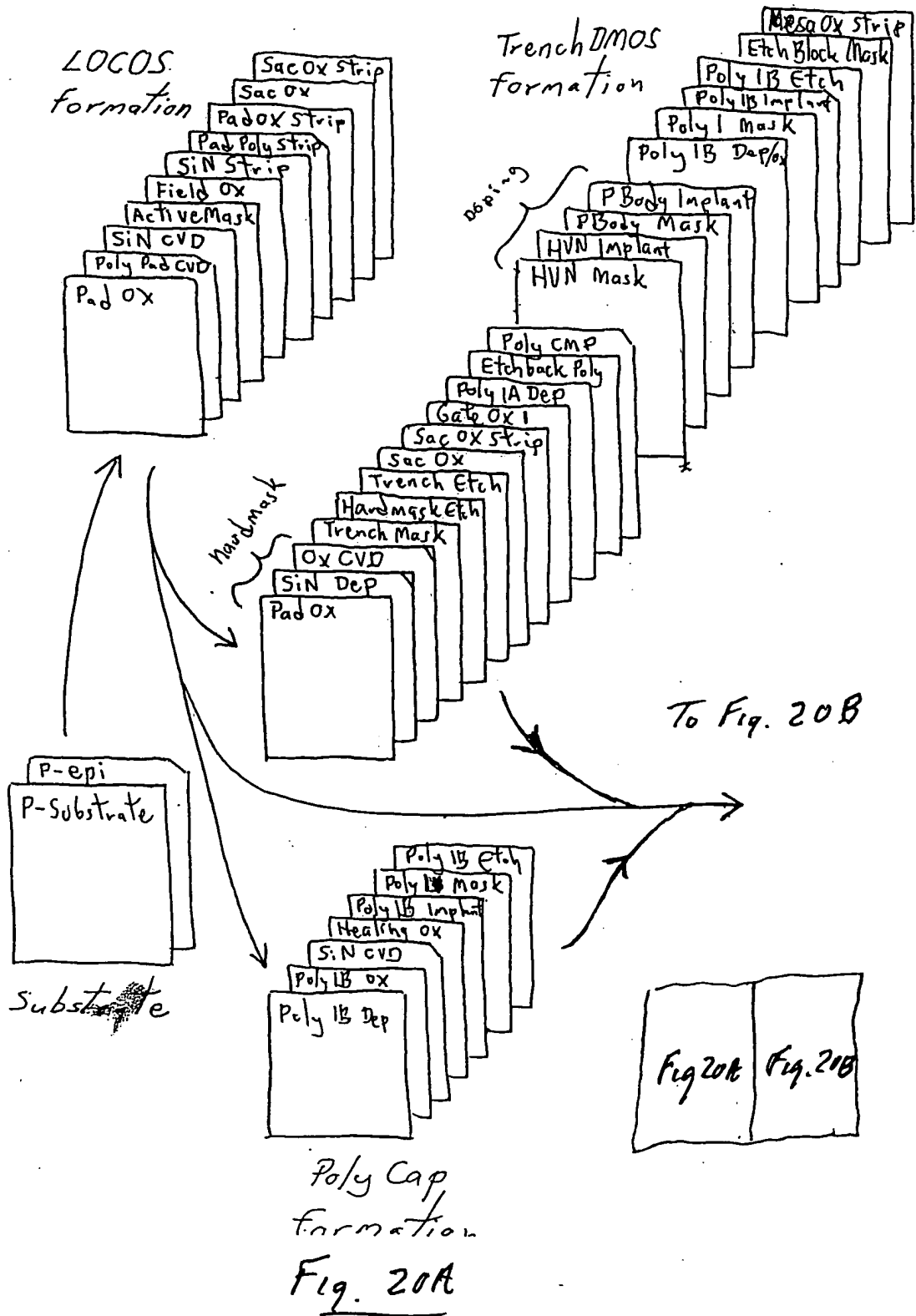


Fig. 19F



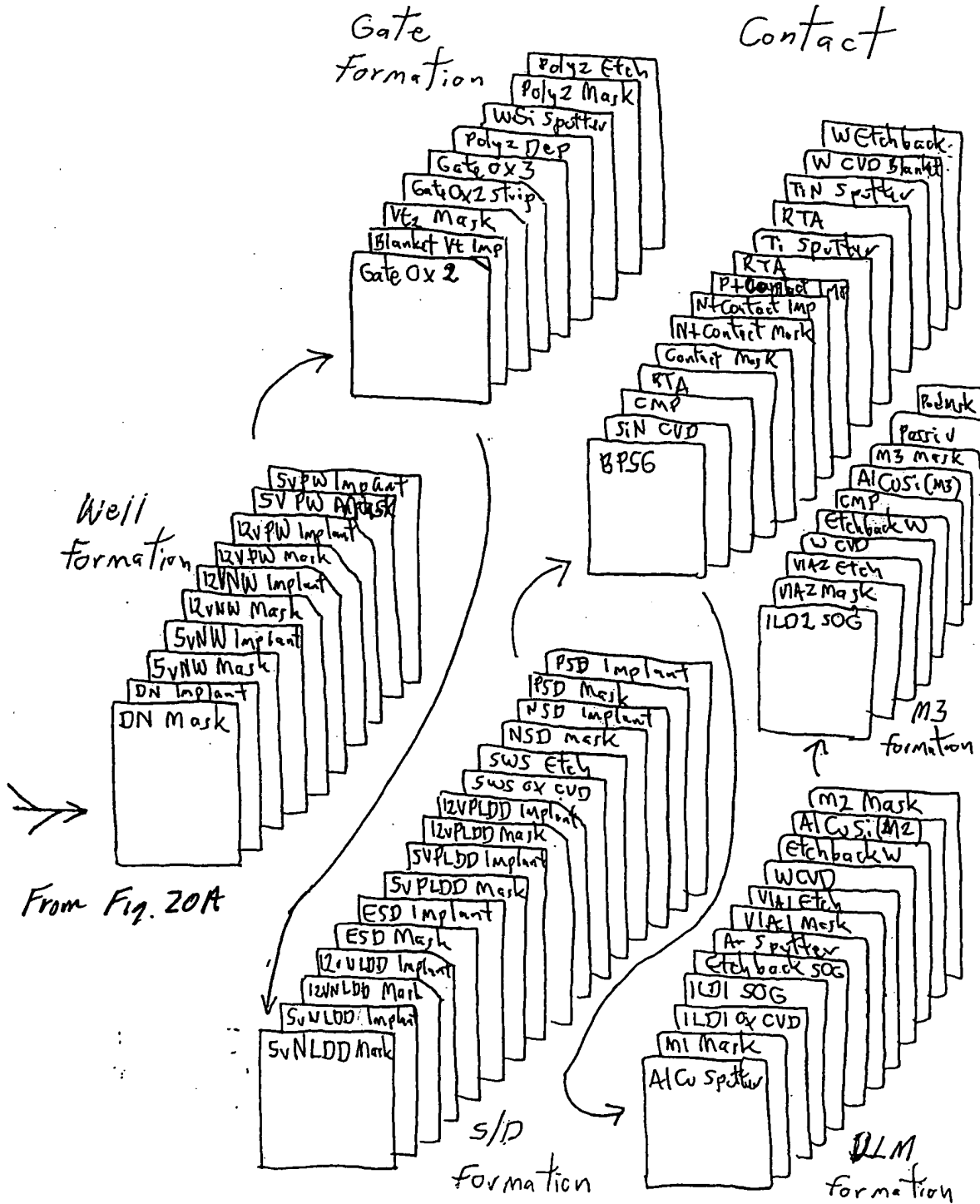


Fig. 20B

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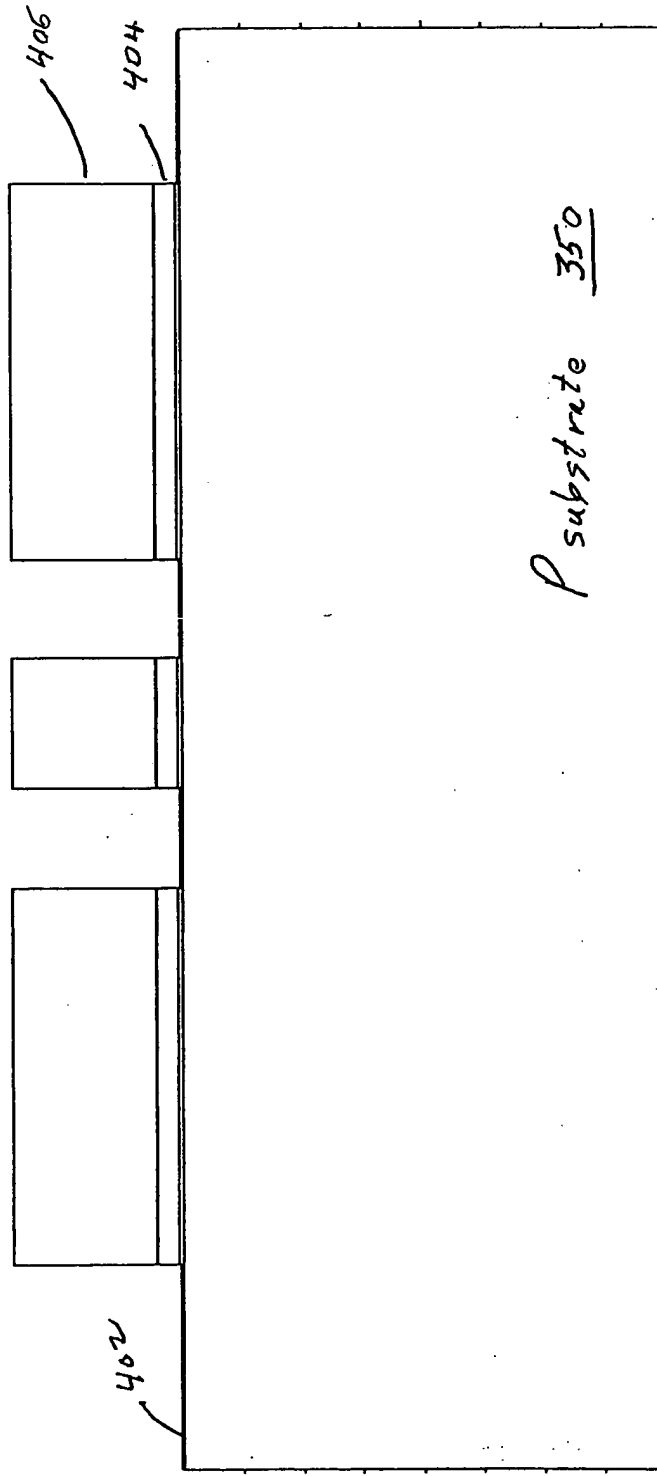
 $P_{\text{substrate}}$  350

First Pad Oxide Layer

Fig. 21

5V PMOS 301

5V NMOS 302

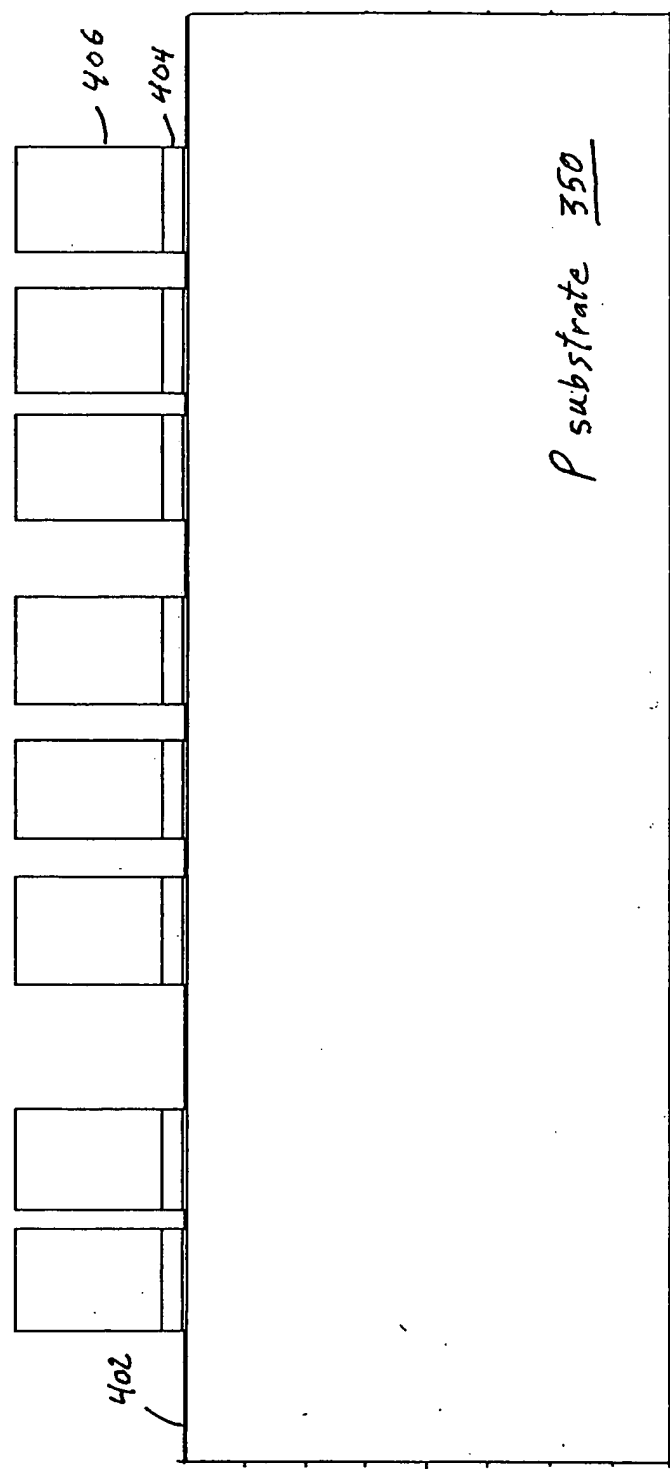


LOCOS - Nitride Mask and Etch

Fig. 22A

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High F<sub>T</sub> Layout  
5V NPN 305      5V PNP 306



Locos - Nitride Mask and Etch

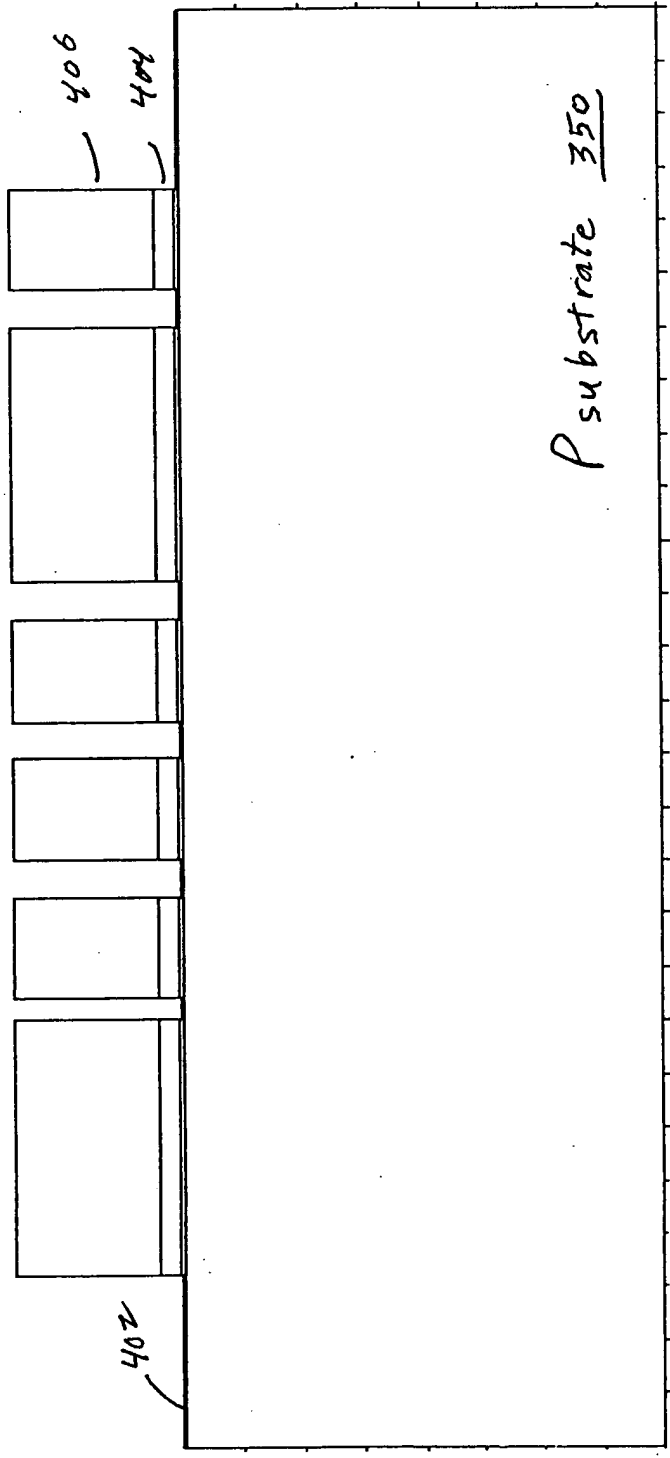
Fig. 22B



Conventional Layout

5V NPN

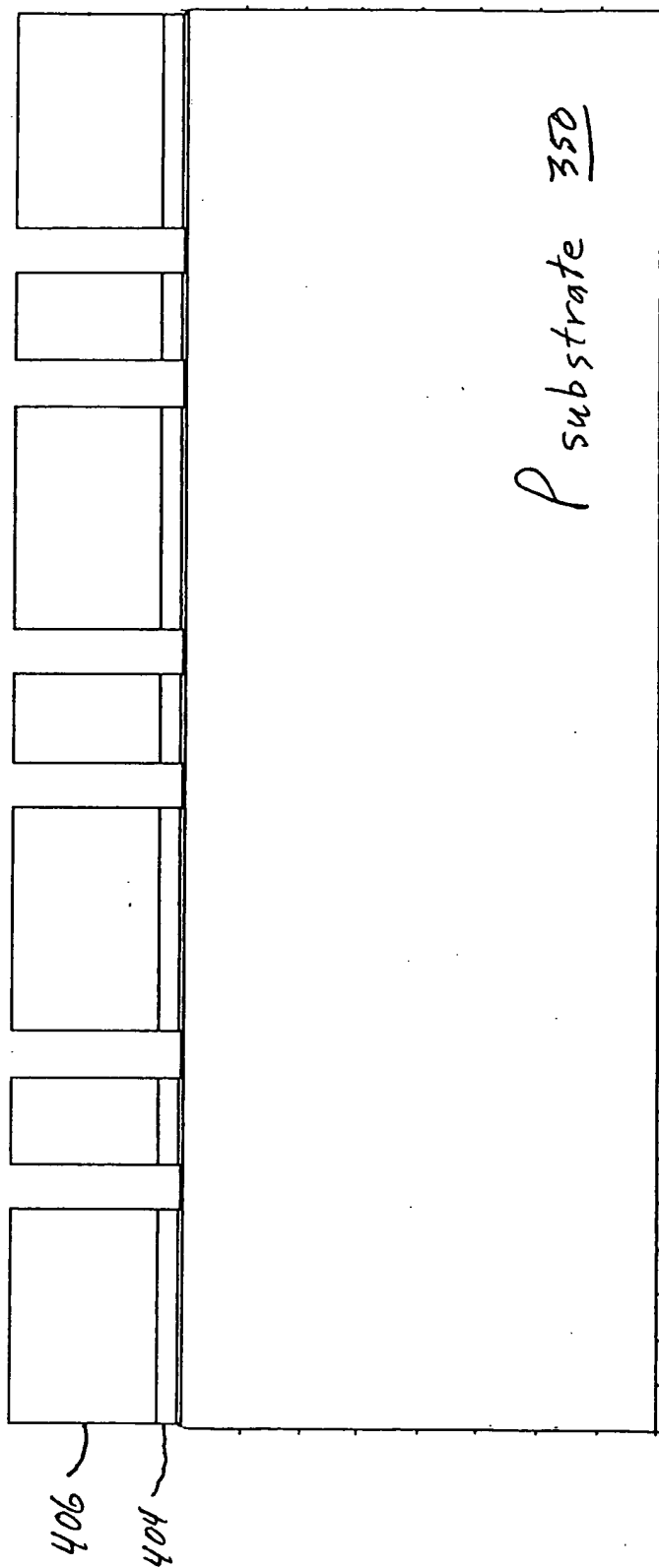
5V PNP



LOCOS - Nitride Mask and Etch

Fig. 22C

30V Lateral Trench DMOS 308



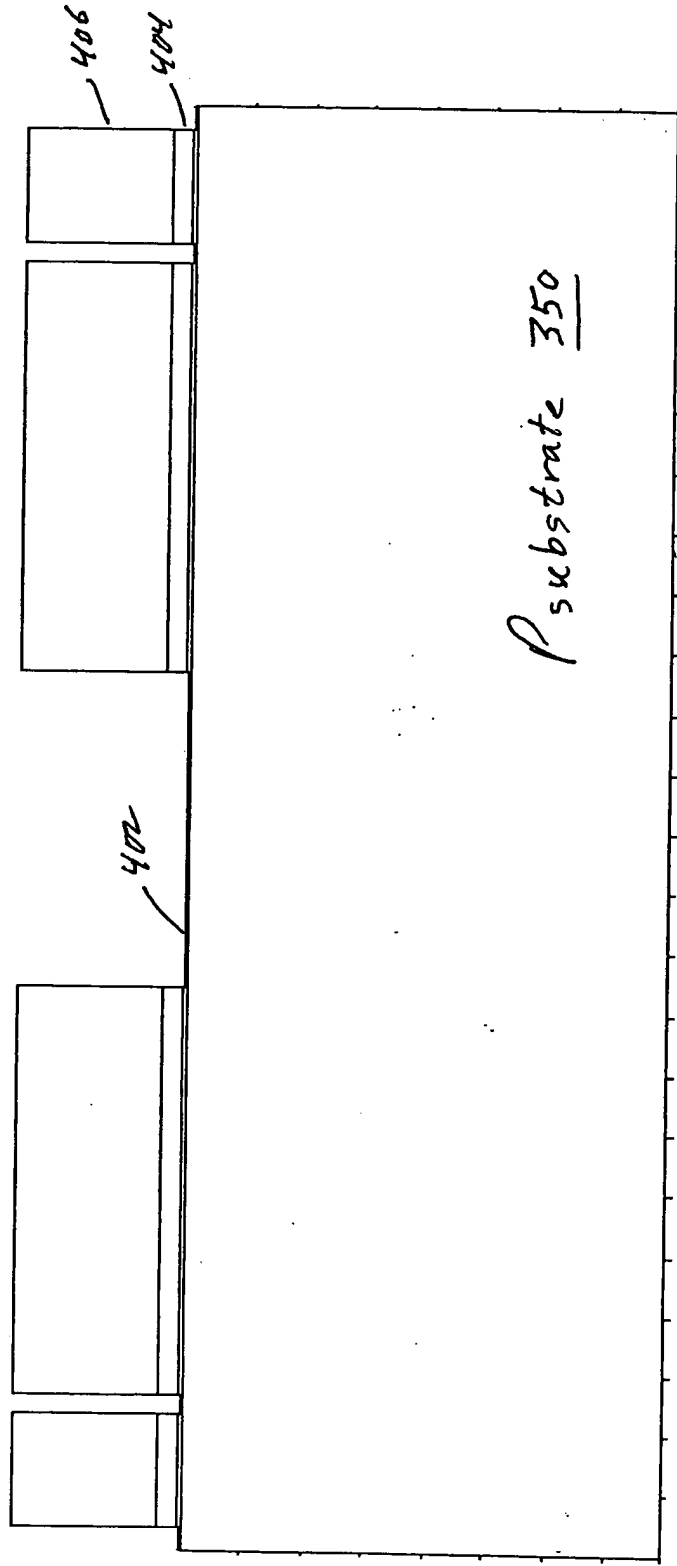
LOCOS - Nitride Mask and Etch

Fig. 22D

Symmetrical 12V CMOS

12V PMOS 309

12V NMOS 310

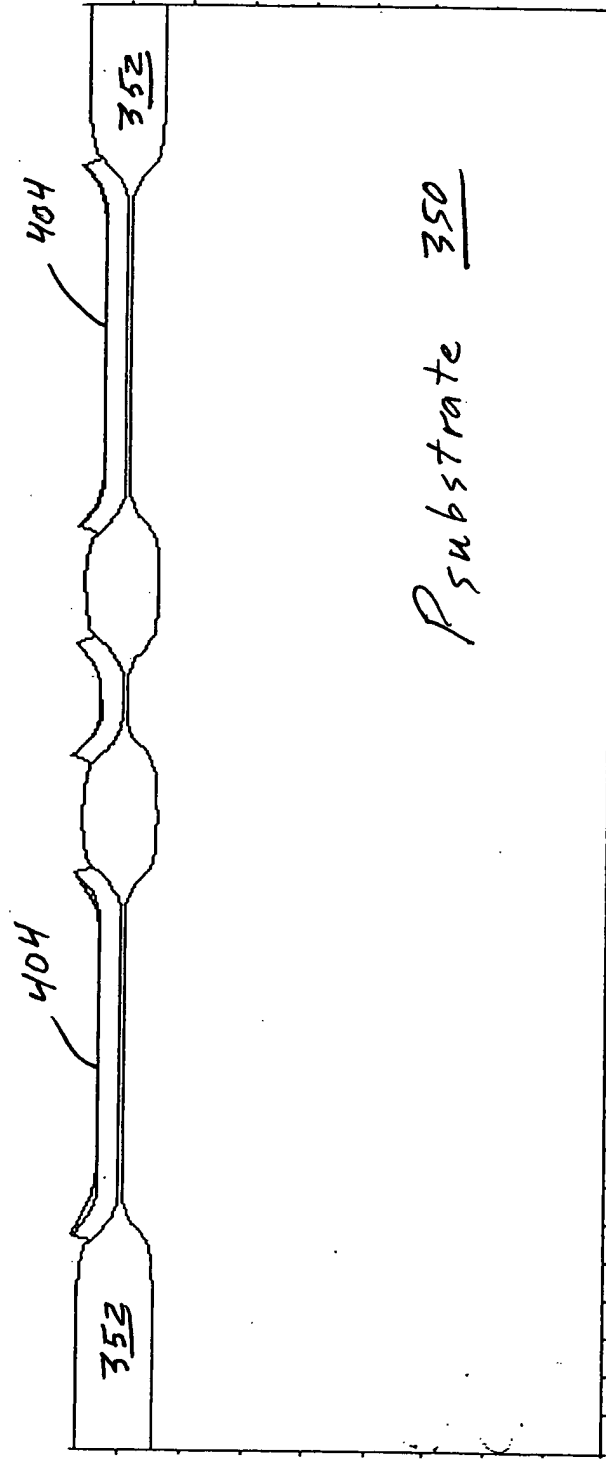


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LOCOS - Nitride Mask and Etch  
Fig. 22E

5V PMOS 301

5V NMOS 302



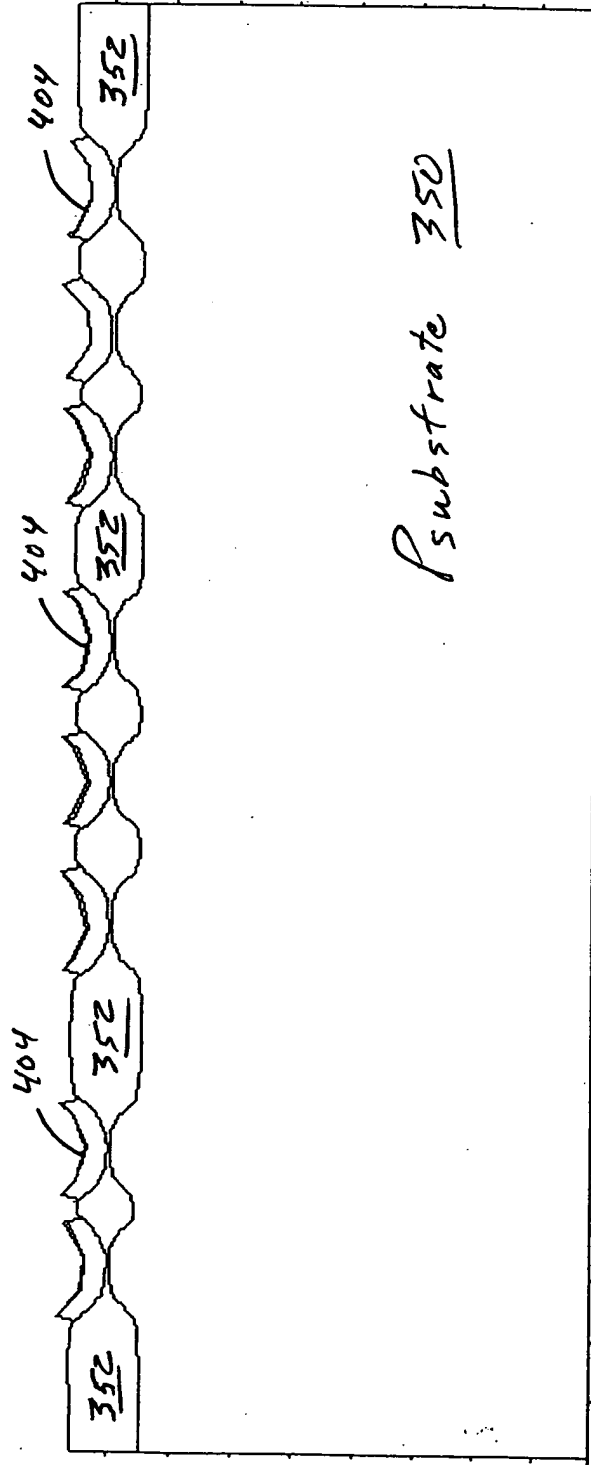
LOCOS - Field Oxidation

Fig. 23A

High F<sub>T</sub> Layout

5V NPN 305

5V PNP 306

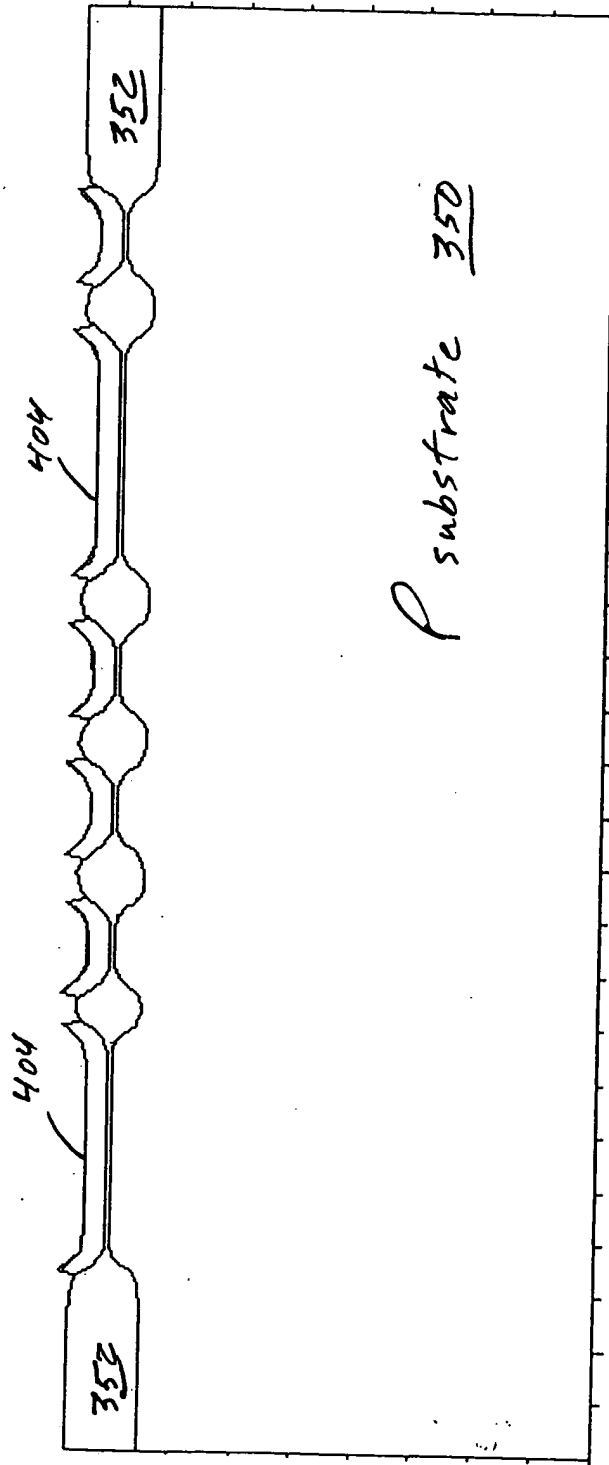


2000s-Field Oxidation

Fig. 23B

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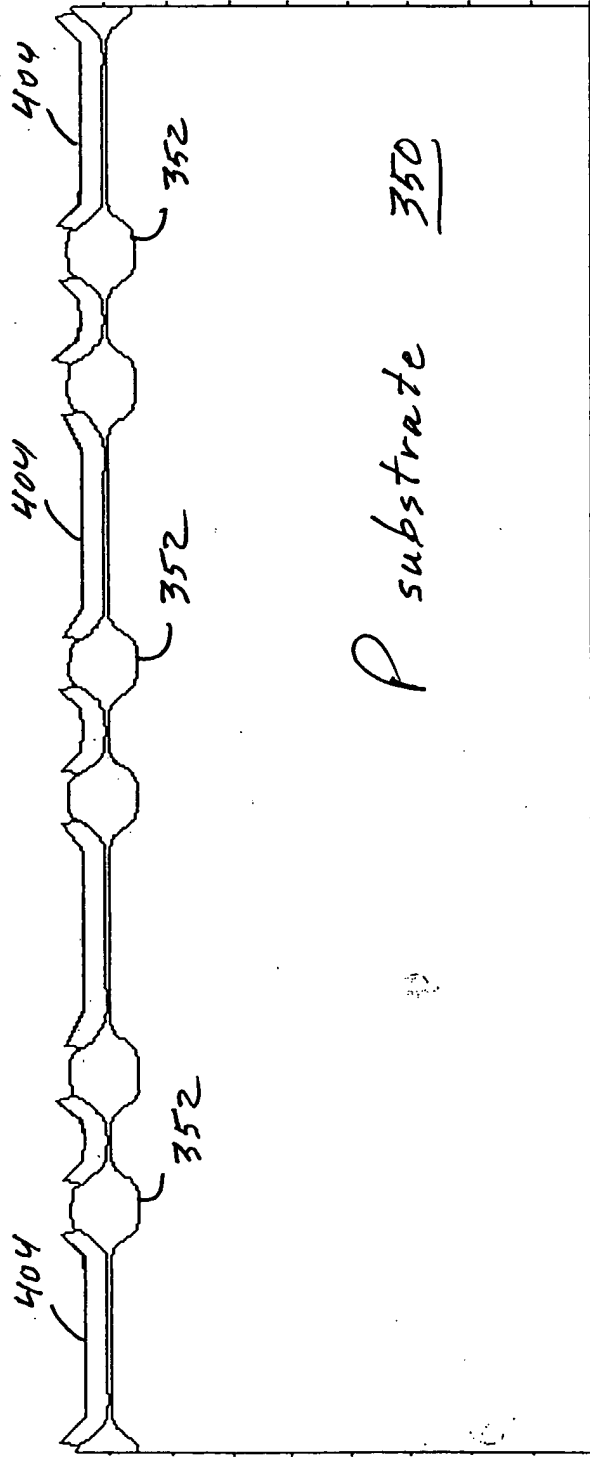
Conventional Layout  
5V NPN      5V PNP



LOCOS-Field Oxidation

Fig 23C

# 30V Latern/ Trench DMOS

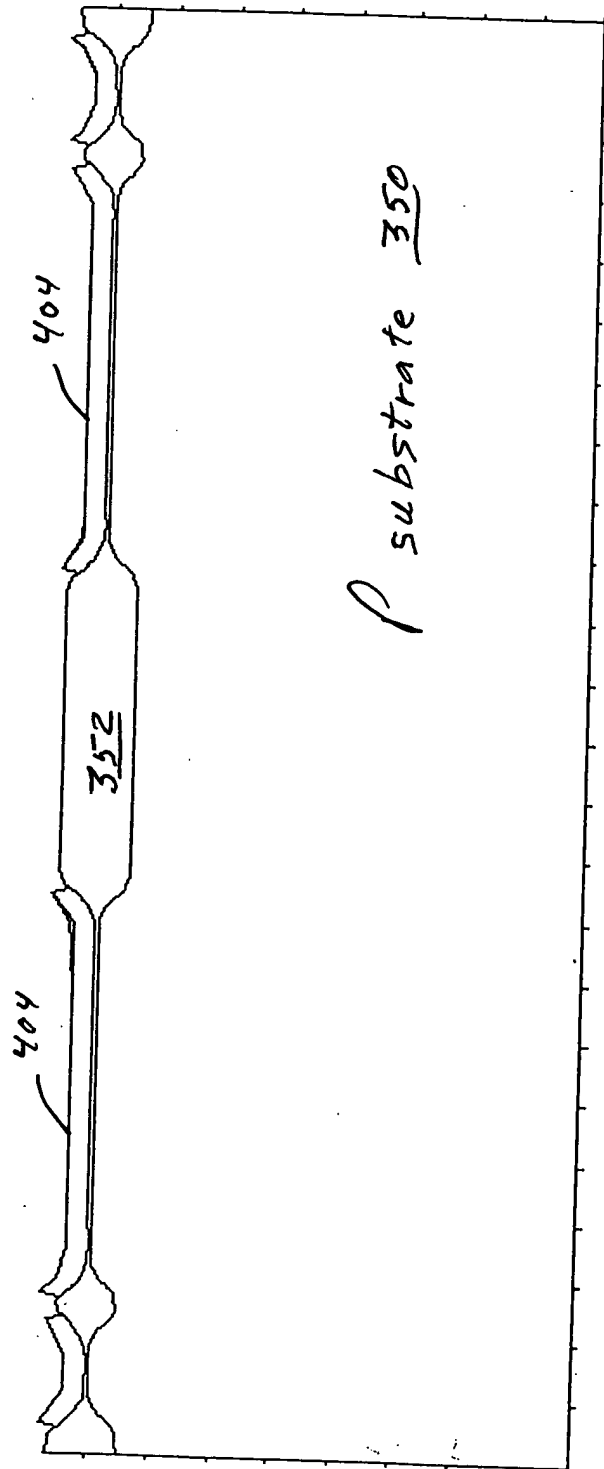


LOCOS - Field Oxidation

Fig. 23D

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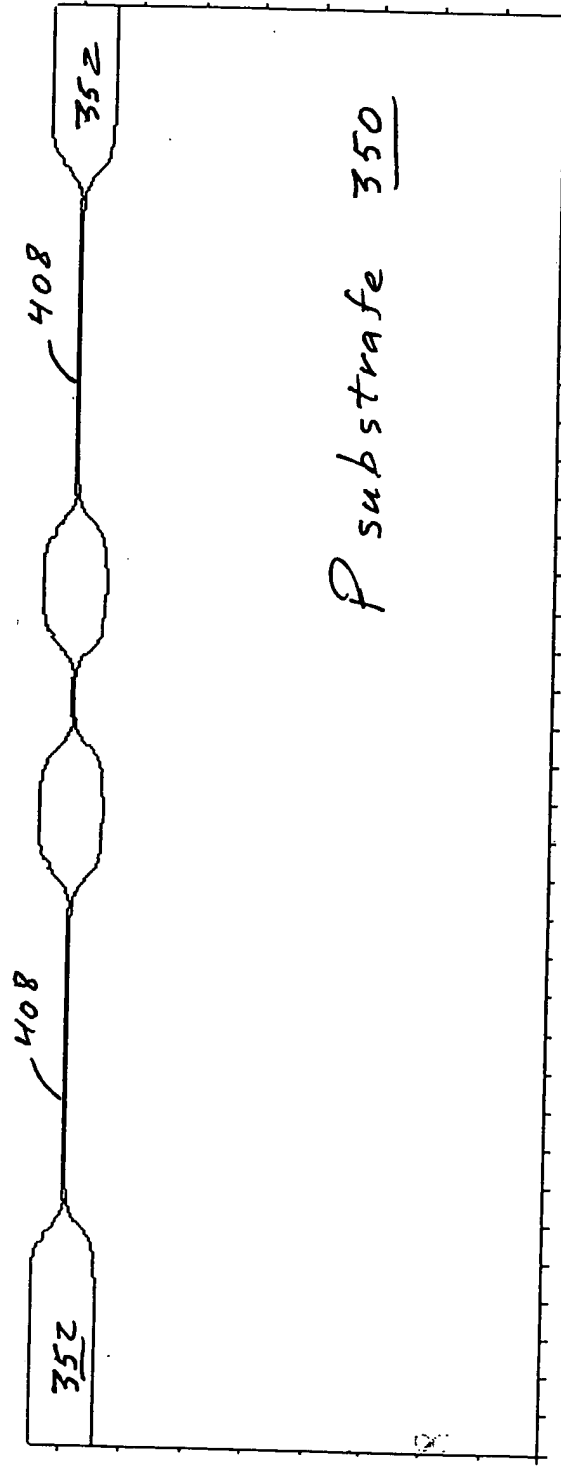
Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



LOCOS - Field Oxidation  
Fig. 23E



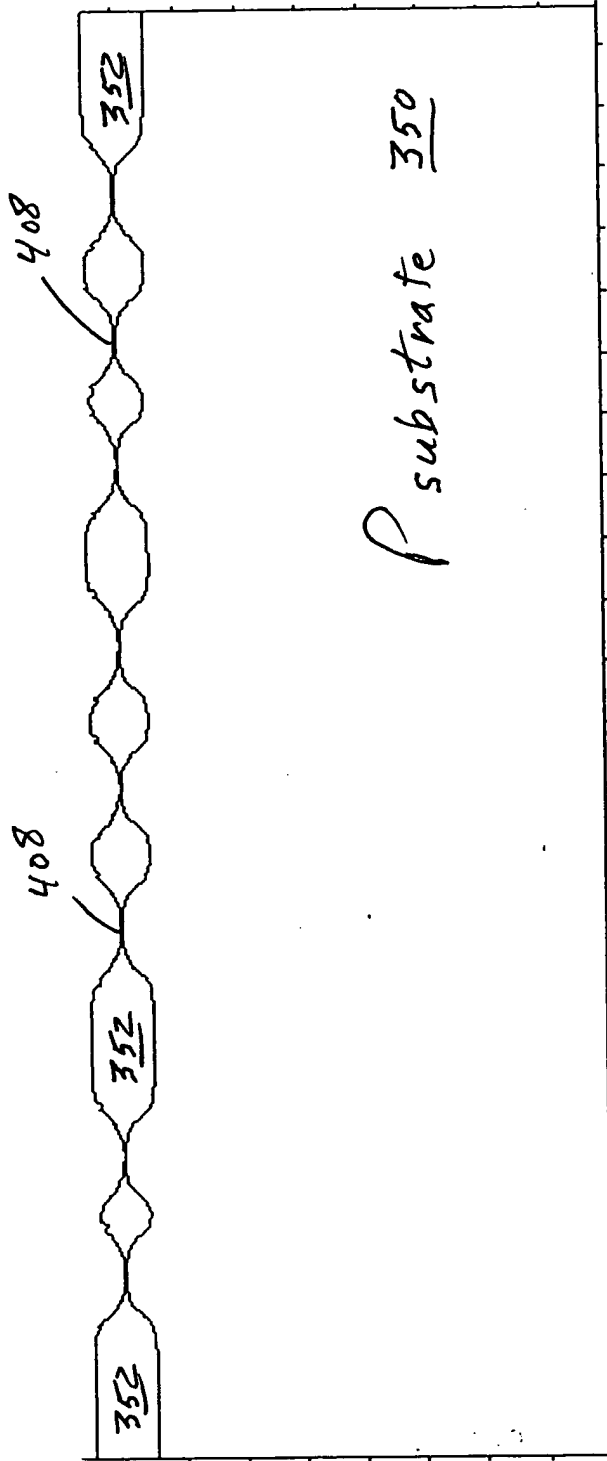
5V PMOS 301      5V NMOS 302



Second Pad Oxide Layer

Fig. 24A

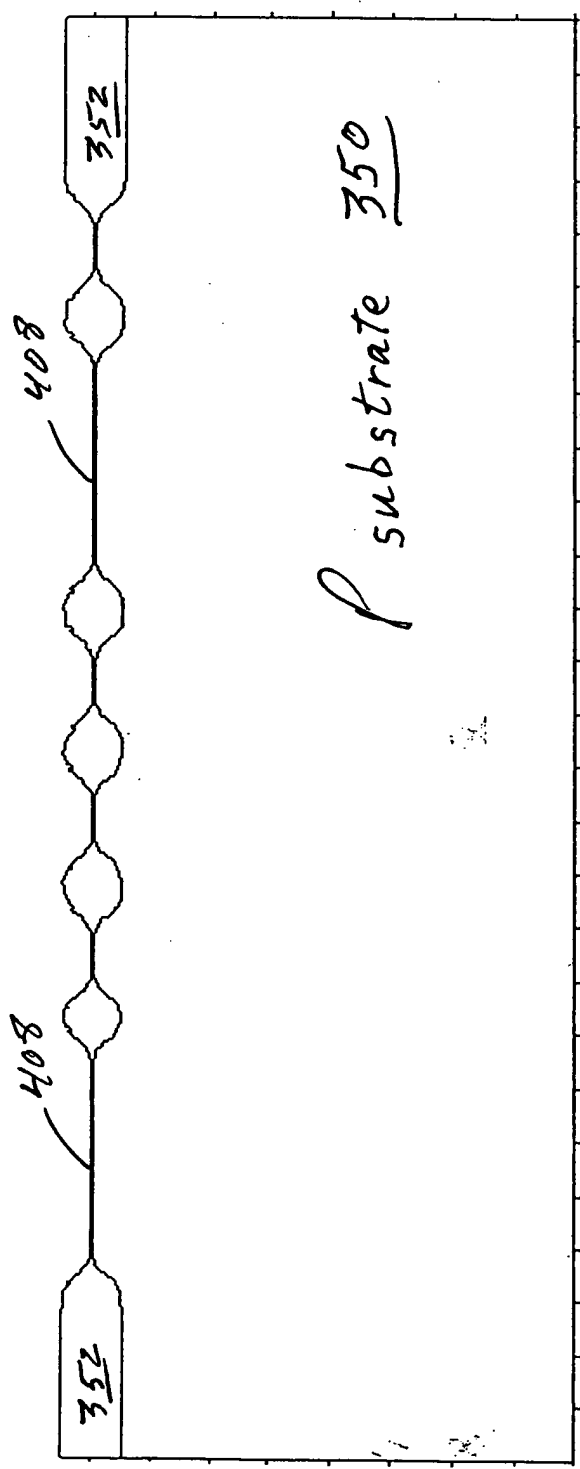
High F<sub>T</sub> Layout  
5V NPN 305      5V PNP 306



Second Pad Oxide Layer

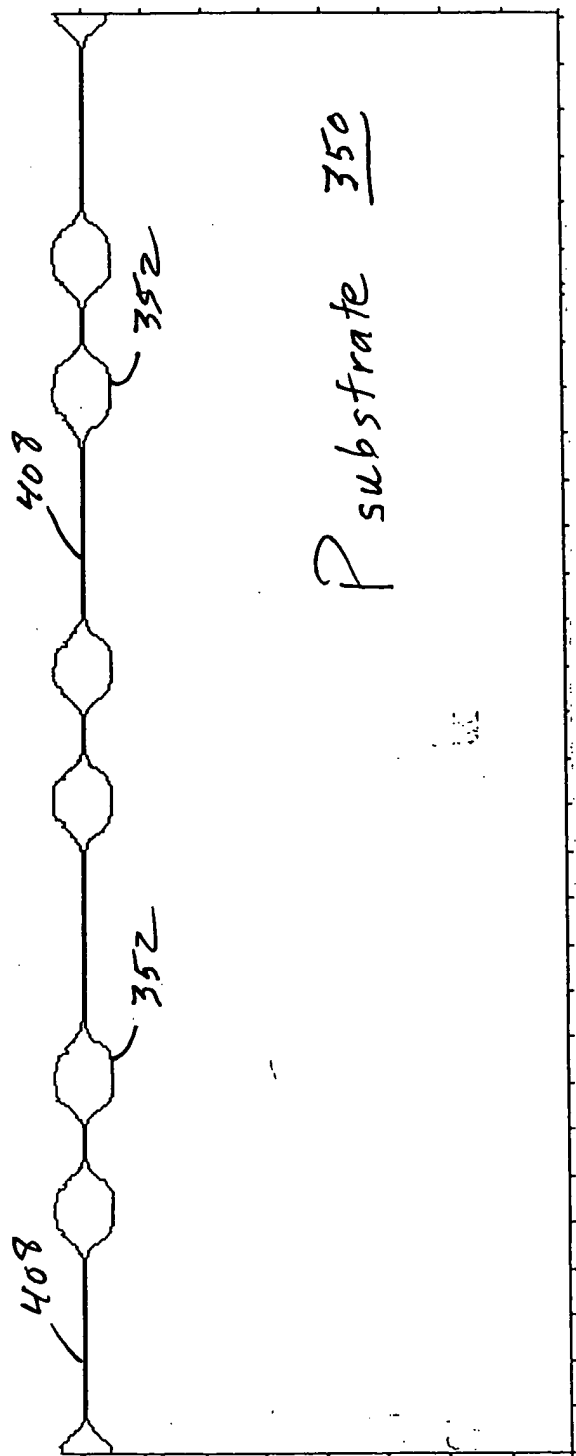
Fig. 24B

Conventional layout  
5V NPN      5V PNP



Second Pad Oxide Layer  
Fig. 24C

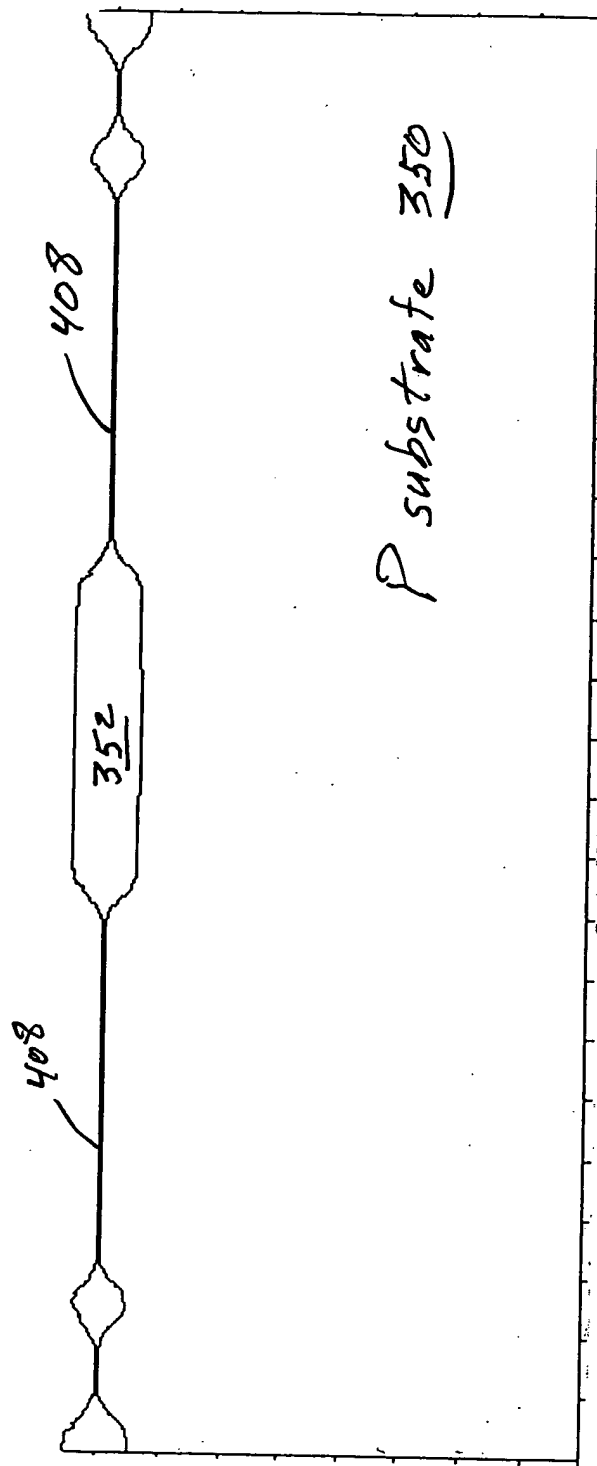
30V Lateral Trench DMOS 308



Second Pad Oxide Layer

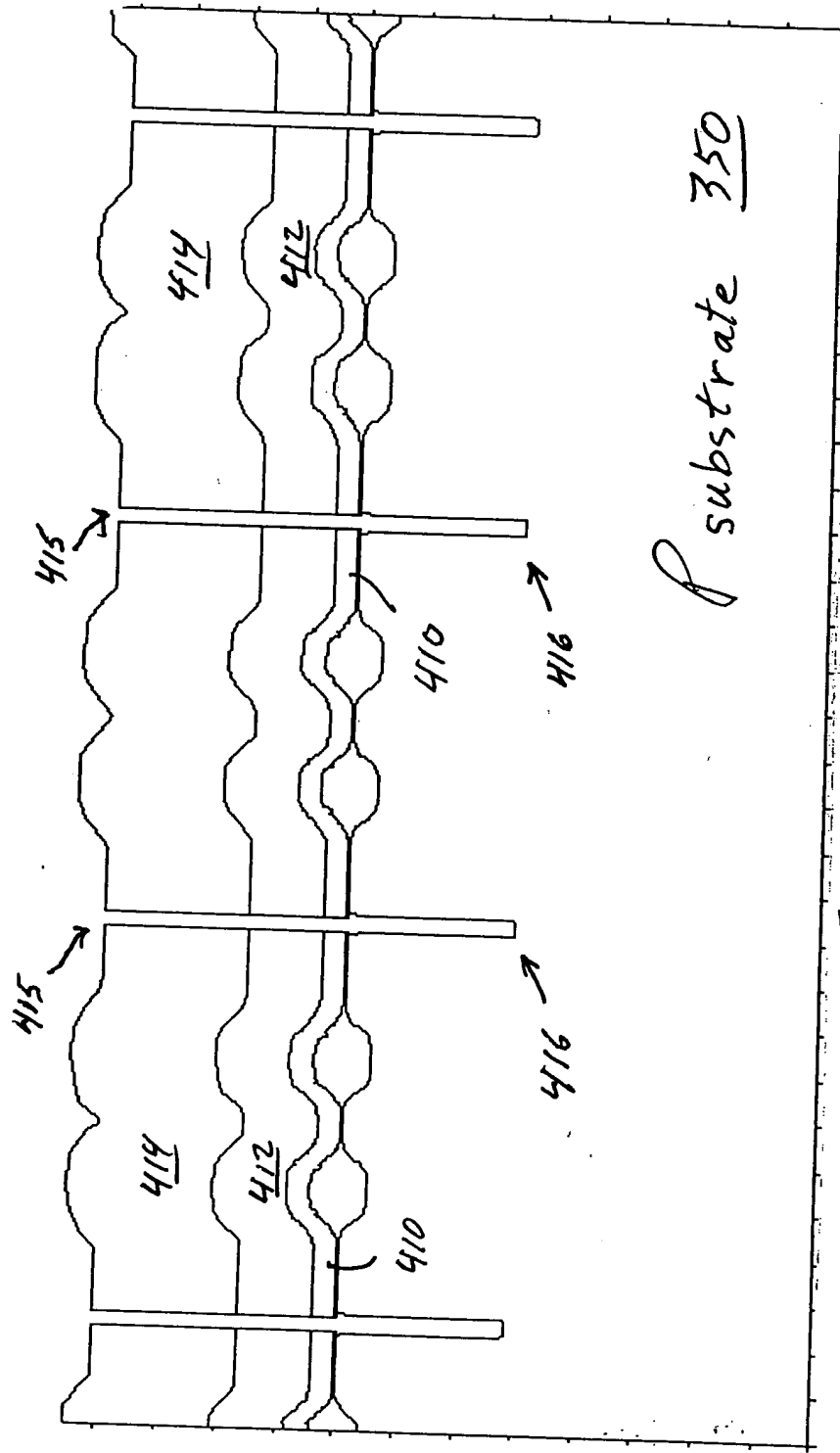
Fig 24D

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



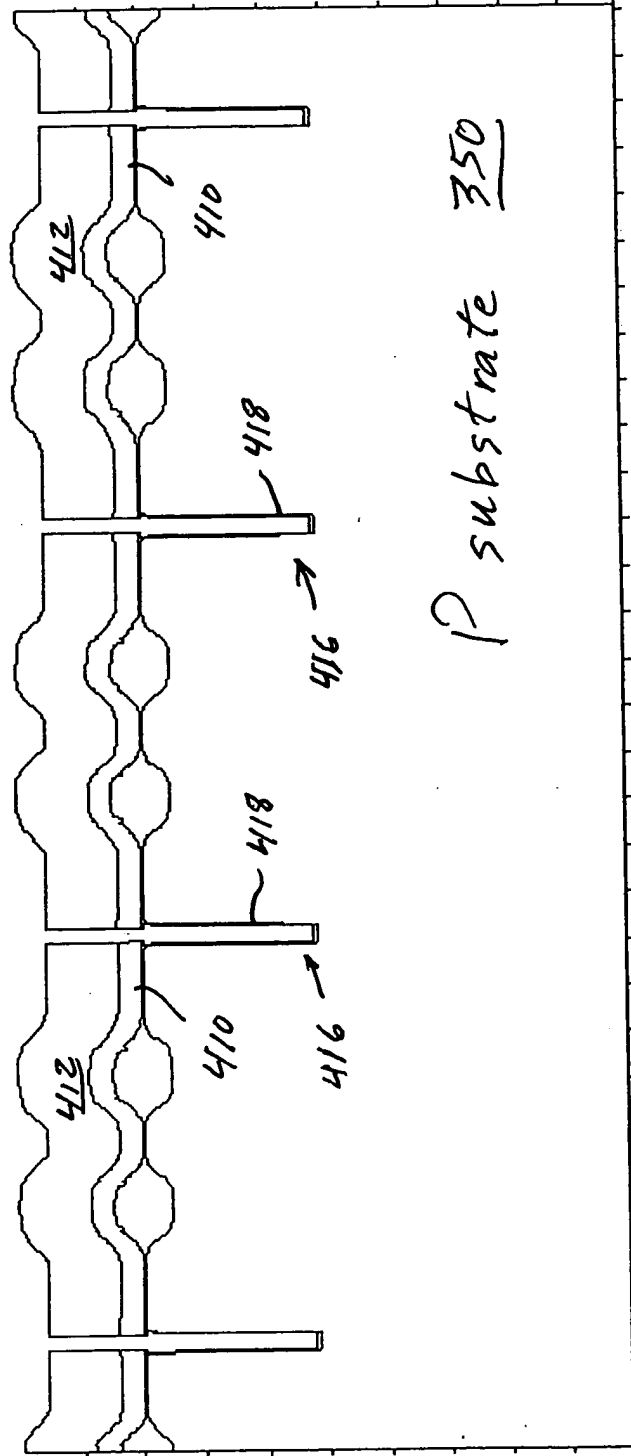
Second Pad Oxide Layer  
Fig. 24E

# 30V Lateral Trench DMOS 308



Trench Hard Mask  
Fig. 25D

# 30V Lateral Trench DMOS 308



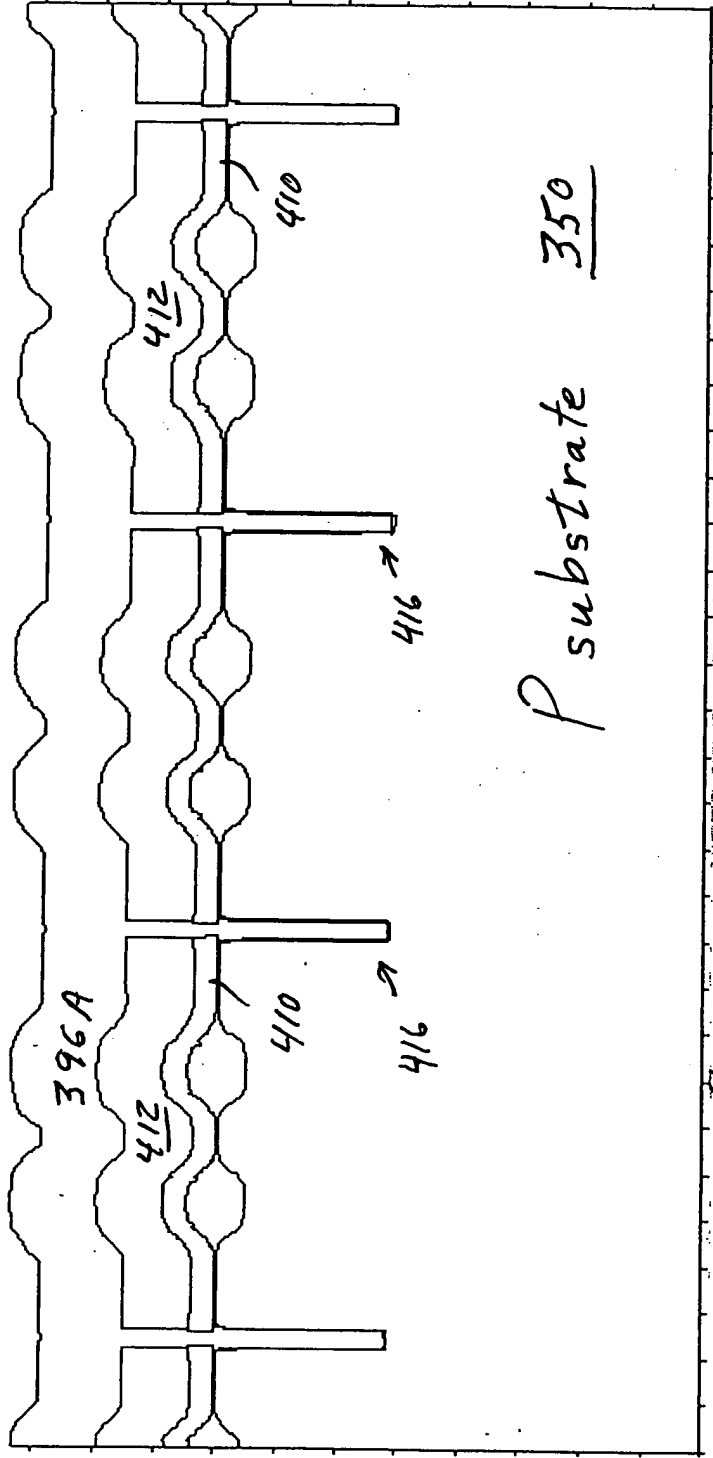
Sacrificial Oxide

Fig. 26D



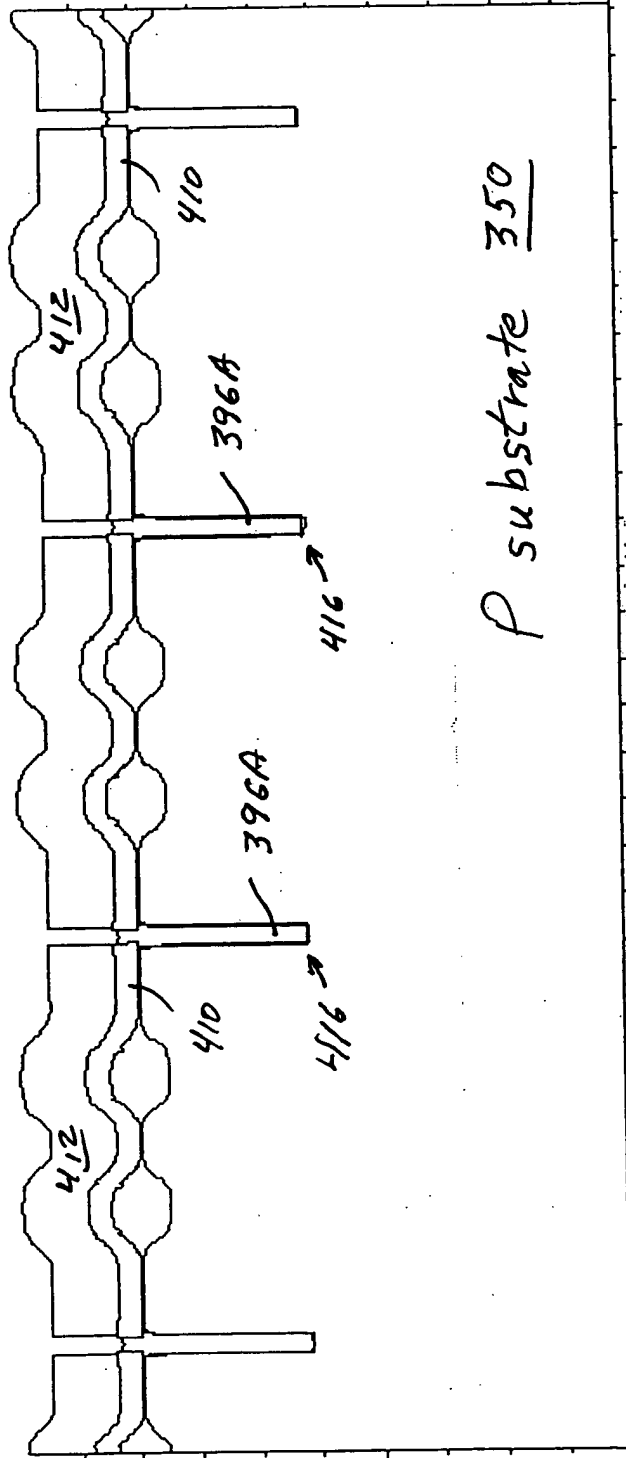


30V Lateral Trench DMOS 308



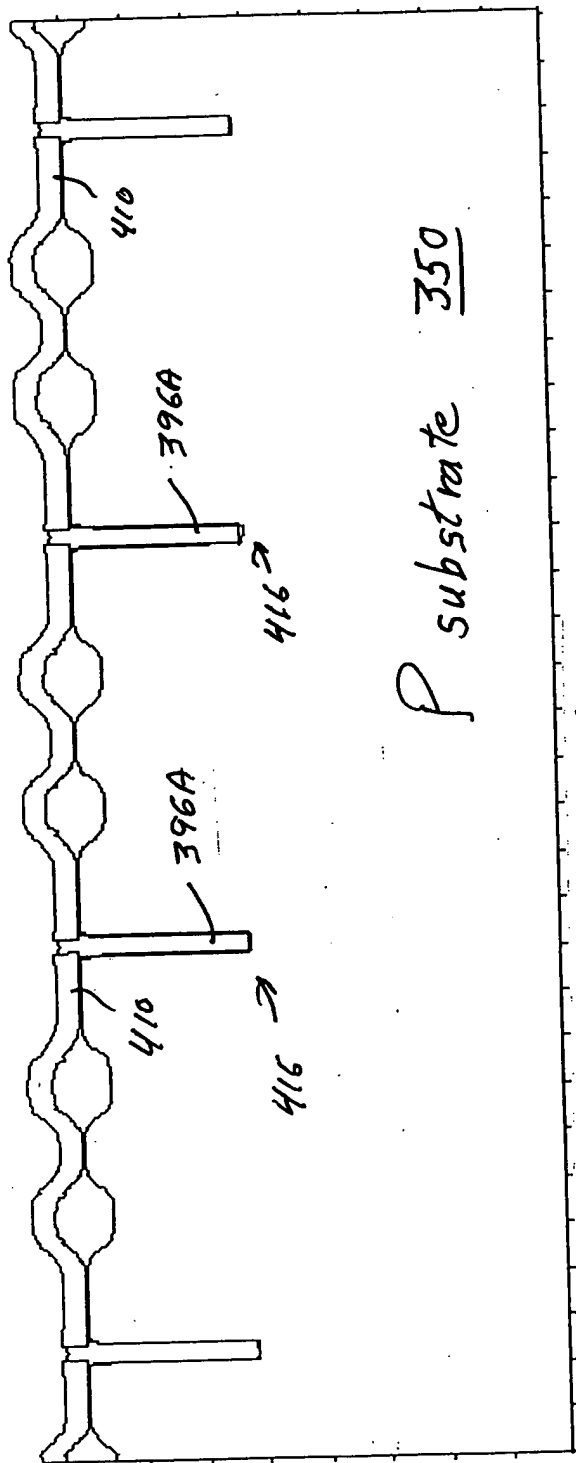
Polysilicon - First Layer  
Fig 28D

# 30V Lateral Trench DMOS 308



Polysilicon Etchback - First Layer  
Fig 29D

# 30V Lateral Trench DMOS 308

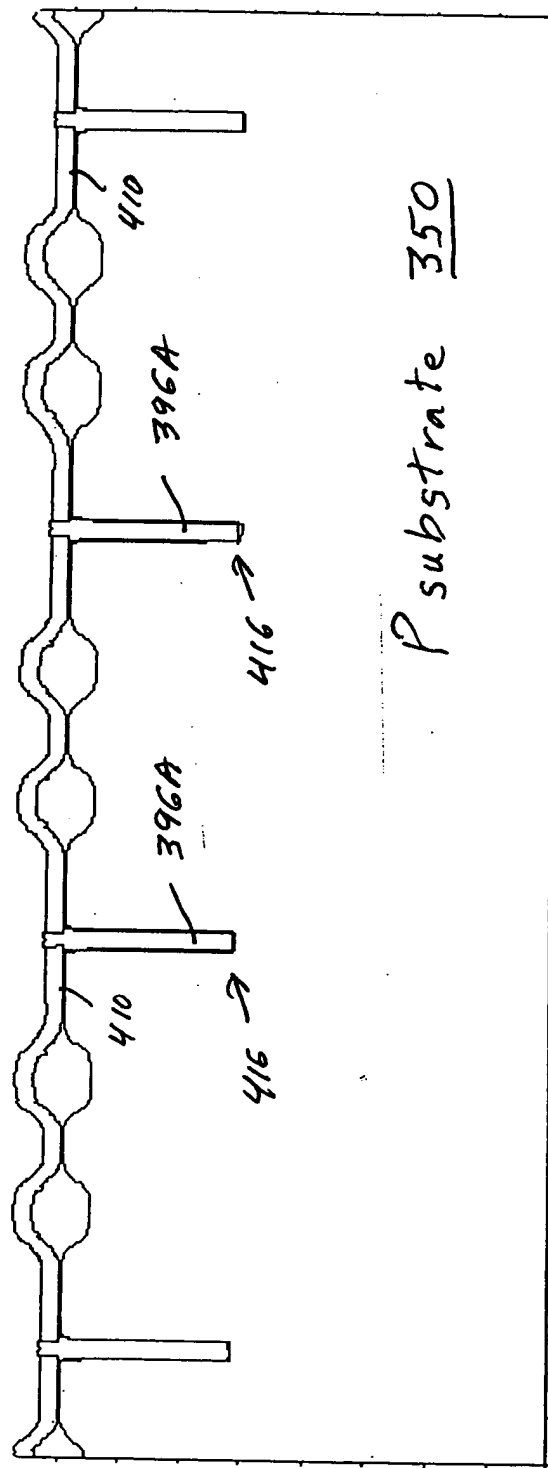


Hard Mask Removal

Fig. 30 D

- 30V Lateral Trench DMOS 308

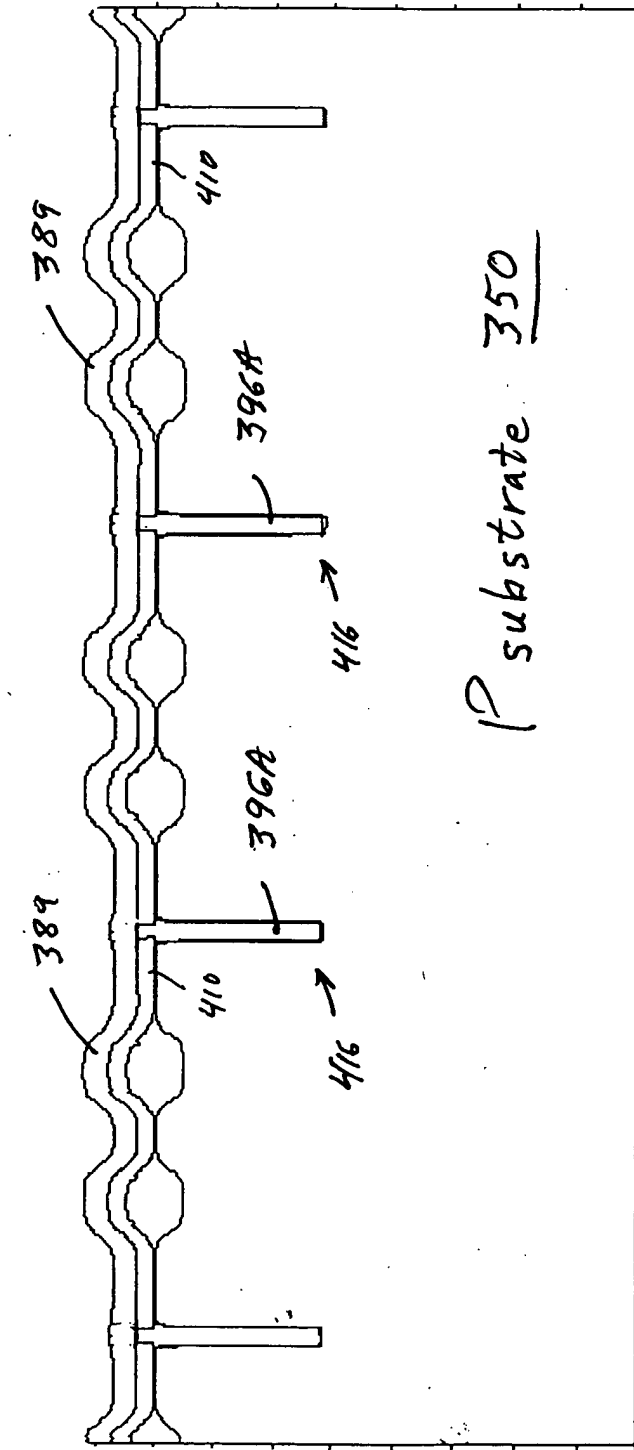
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Second Polysilicon Etchback - First Layer

Fig. 31D

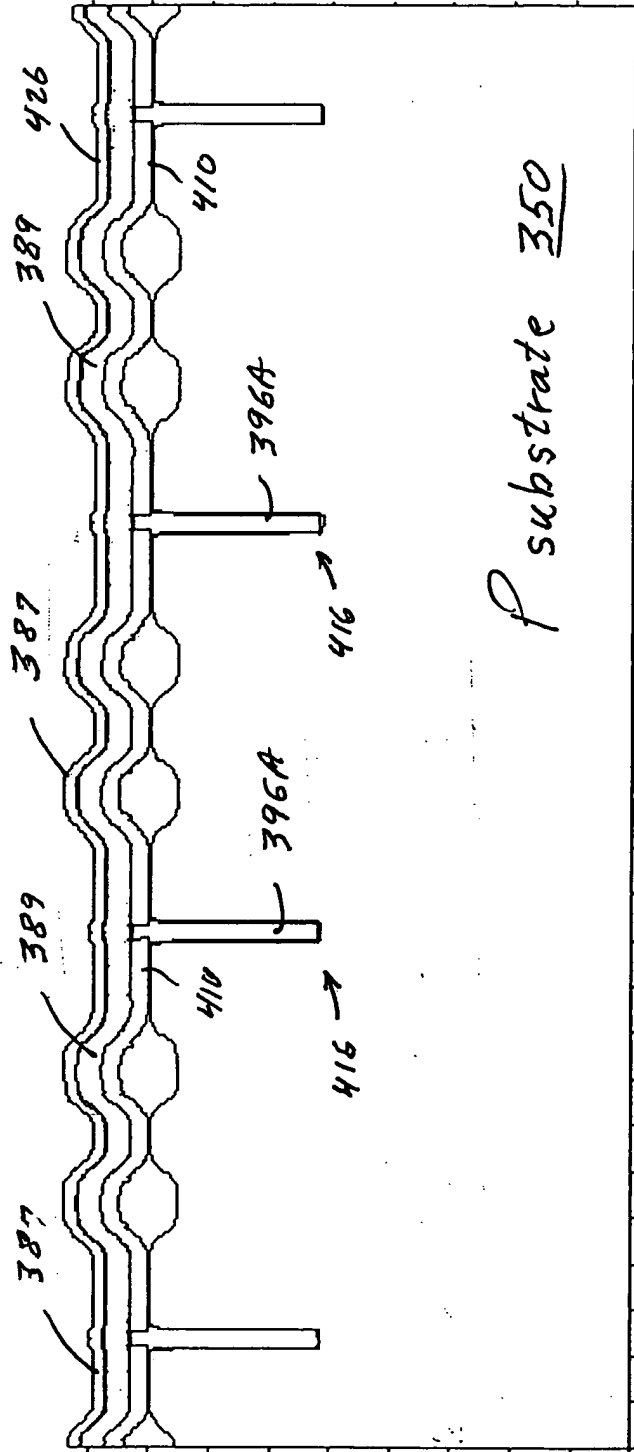
# 30V Lateral Trench DMOS 308



Polysilicon - Second Layer  
Fig. 32D

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# 30V Lateral Trench DMOS 308



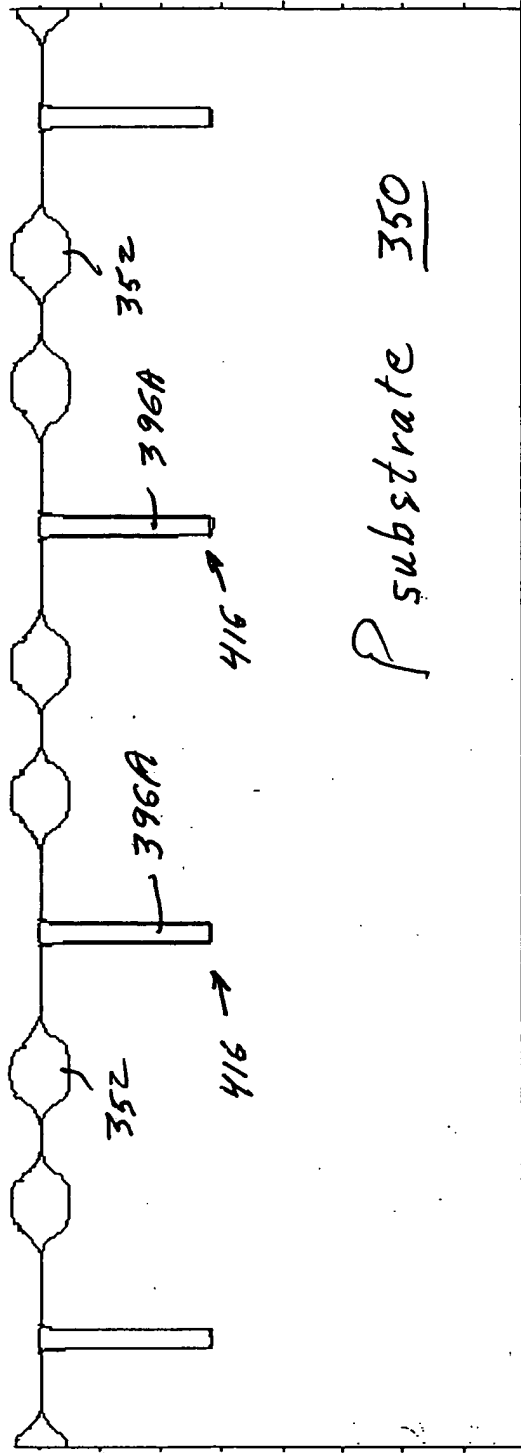
P substrate 350

Interlayer Dielectric

Fig. 33D

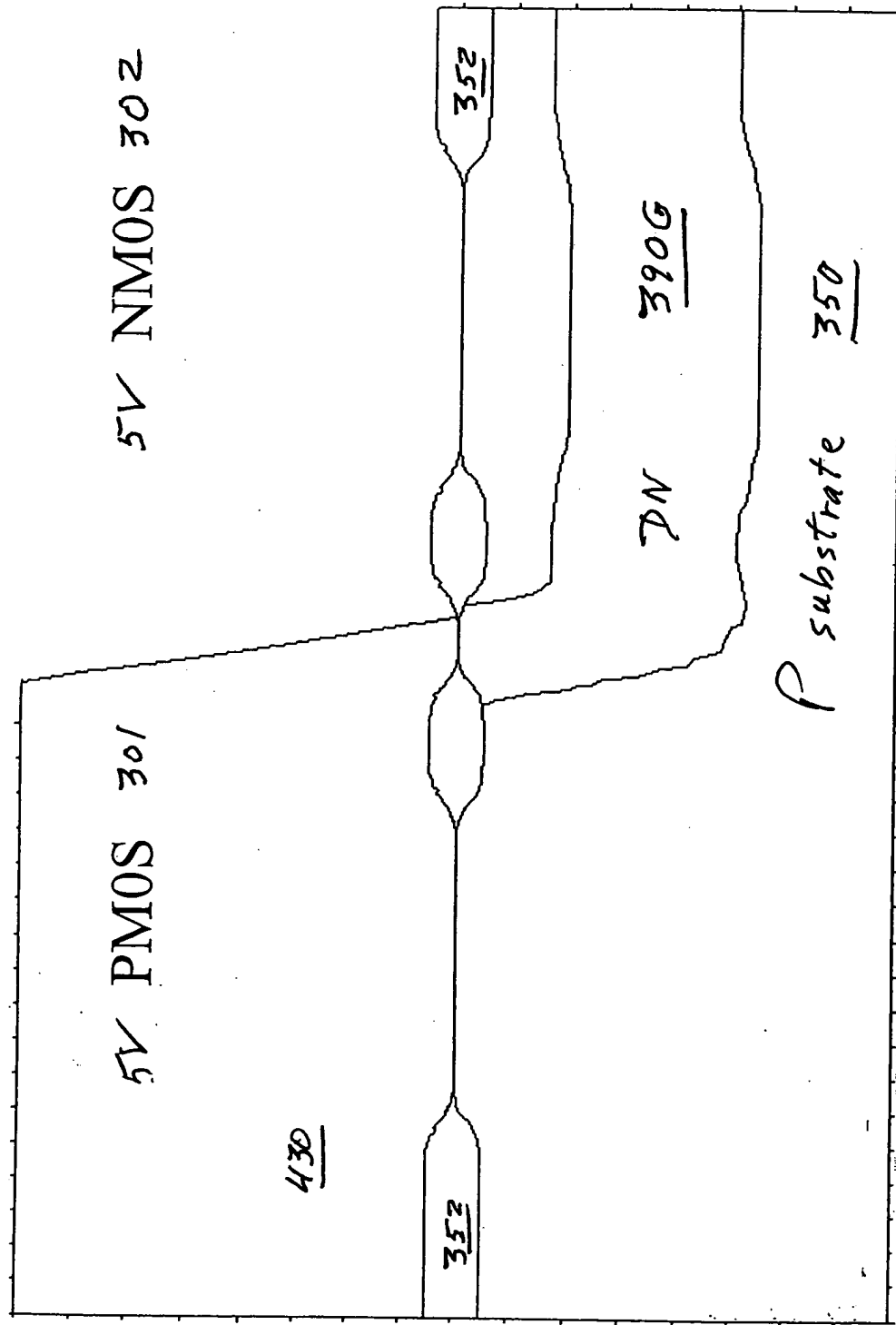
# 30 V Lateral Trench DMOS 308

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Etch back - Inter-layer Dielectric and Second Poly

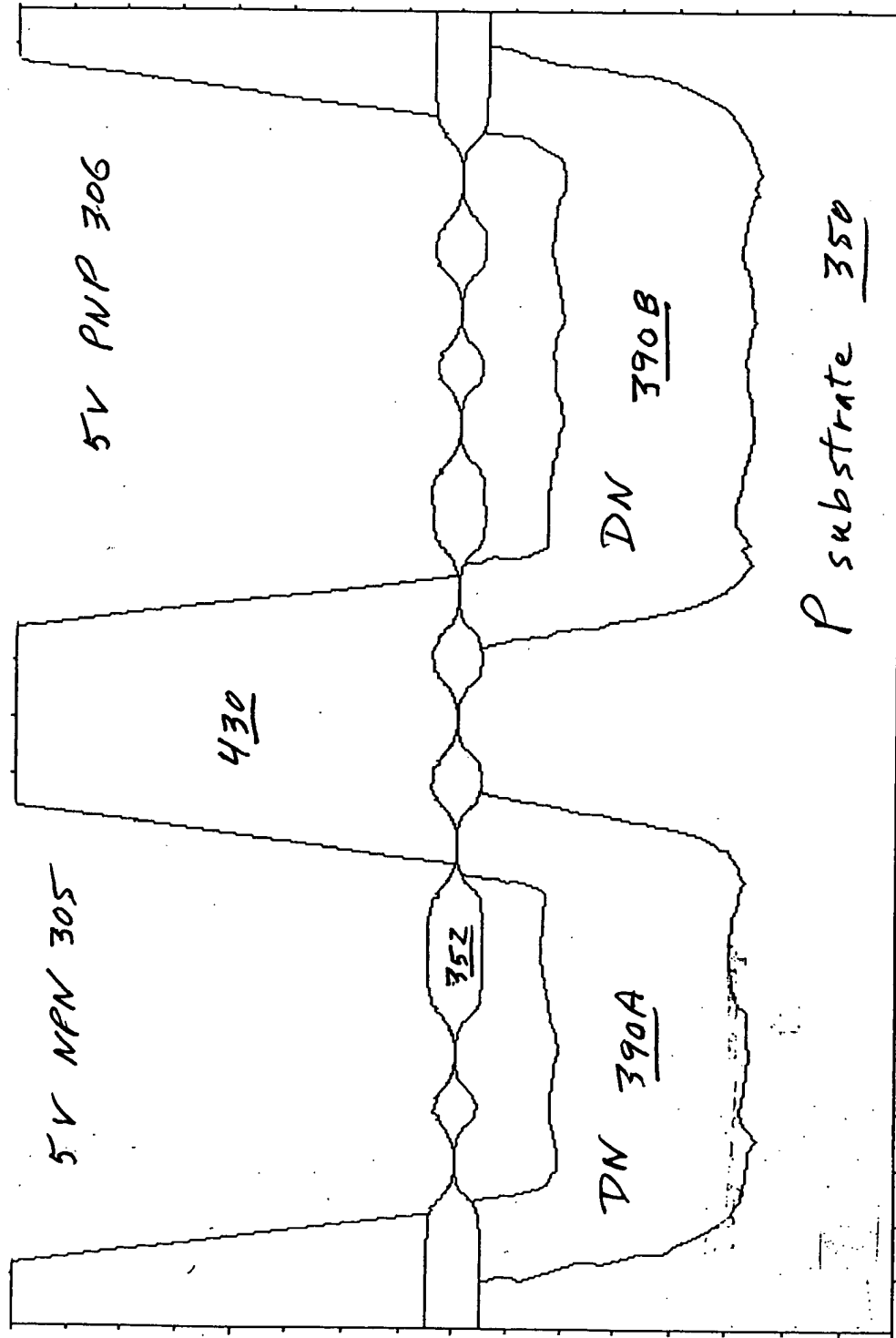
Fig. 34D



Deep N Mask and Implant  
Fig. 35A

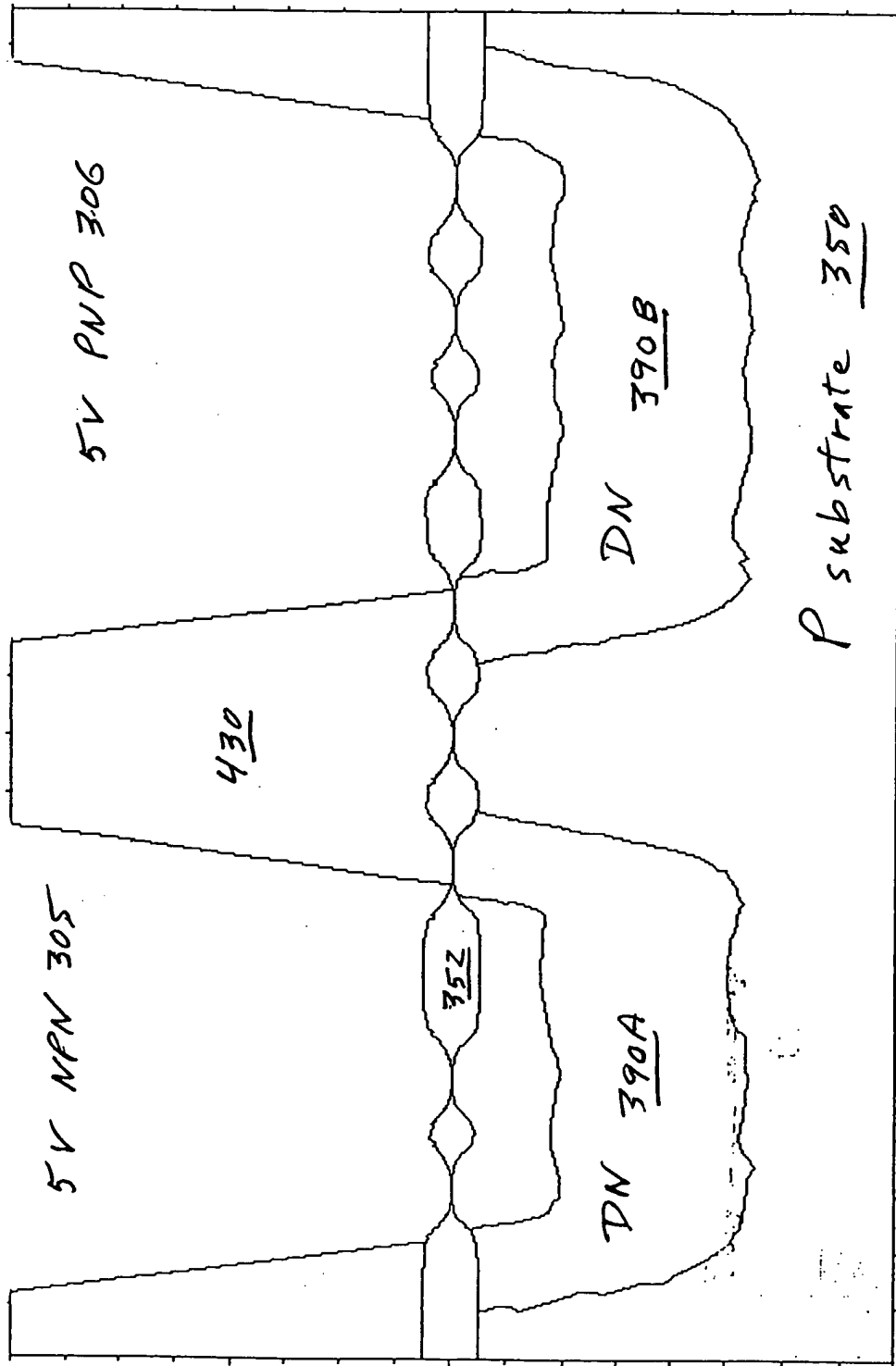
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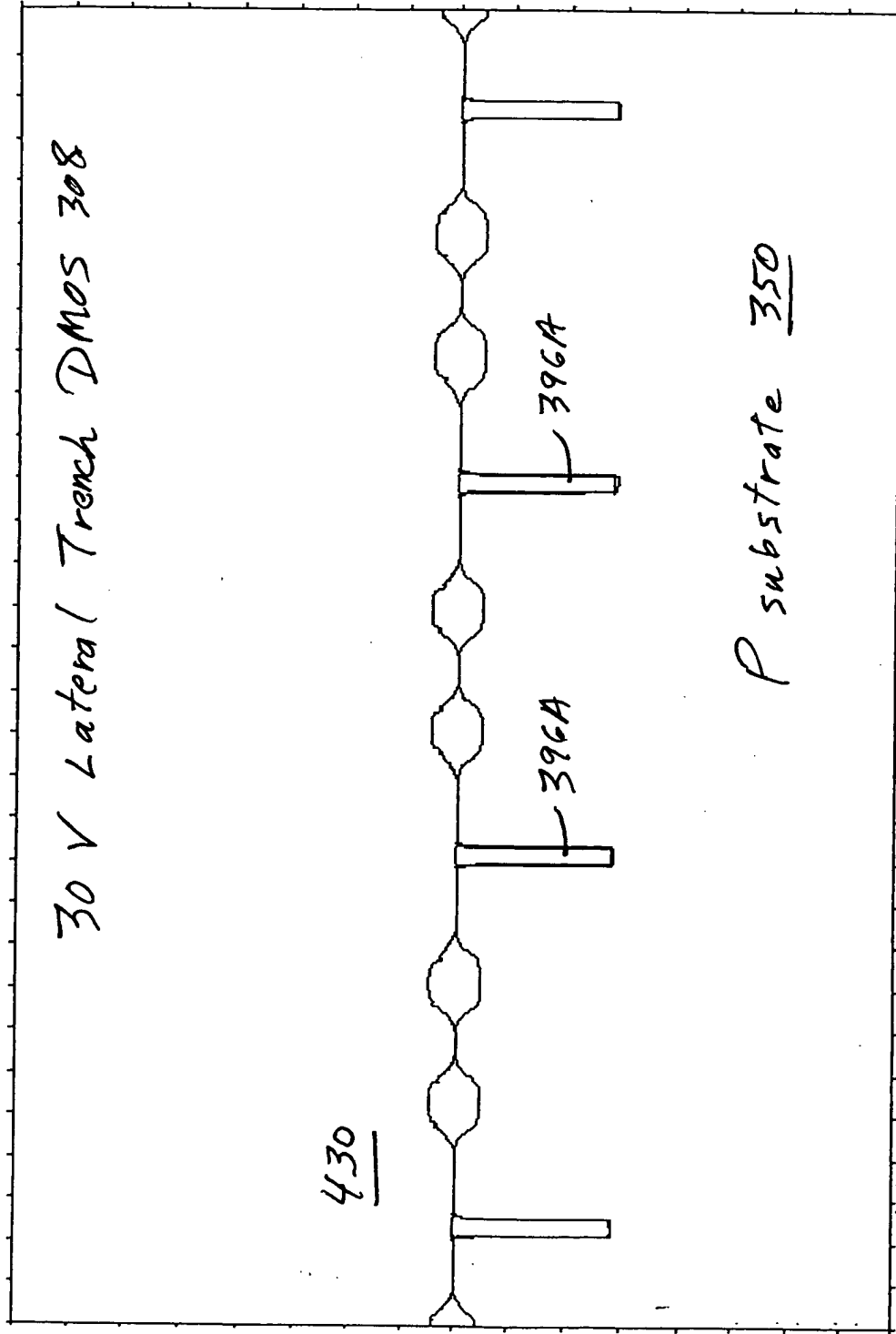
High  $F_T$  LayoutDeep N Mask and Implant  
Fig 35B

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Conventional Layout



Deep N Mask and Implant  
Fig. 35C

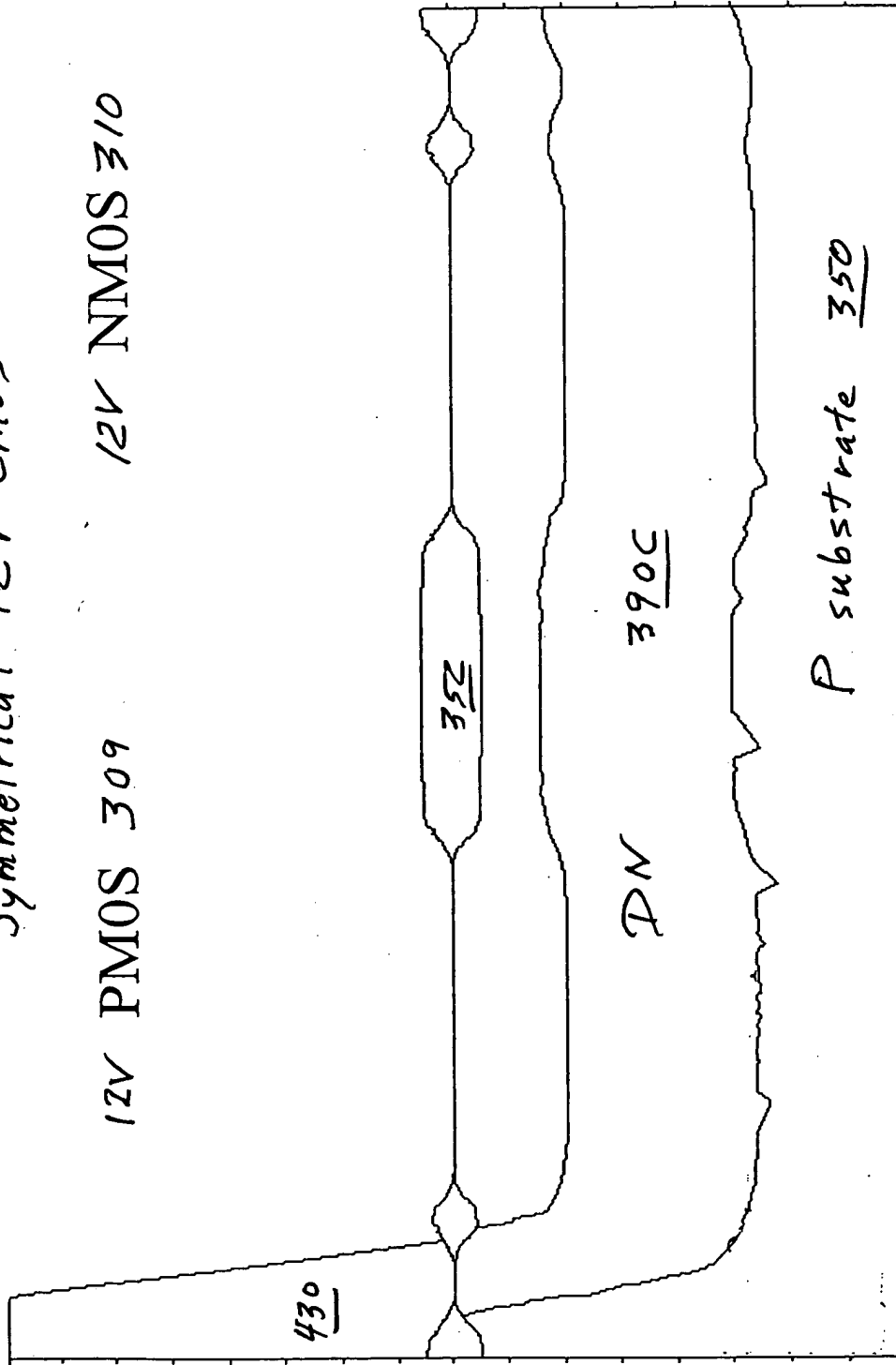


Deep N Mask and Implant  
Fig. 35D

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Symmetrical 12V CMOS

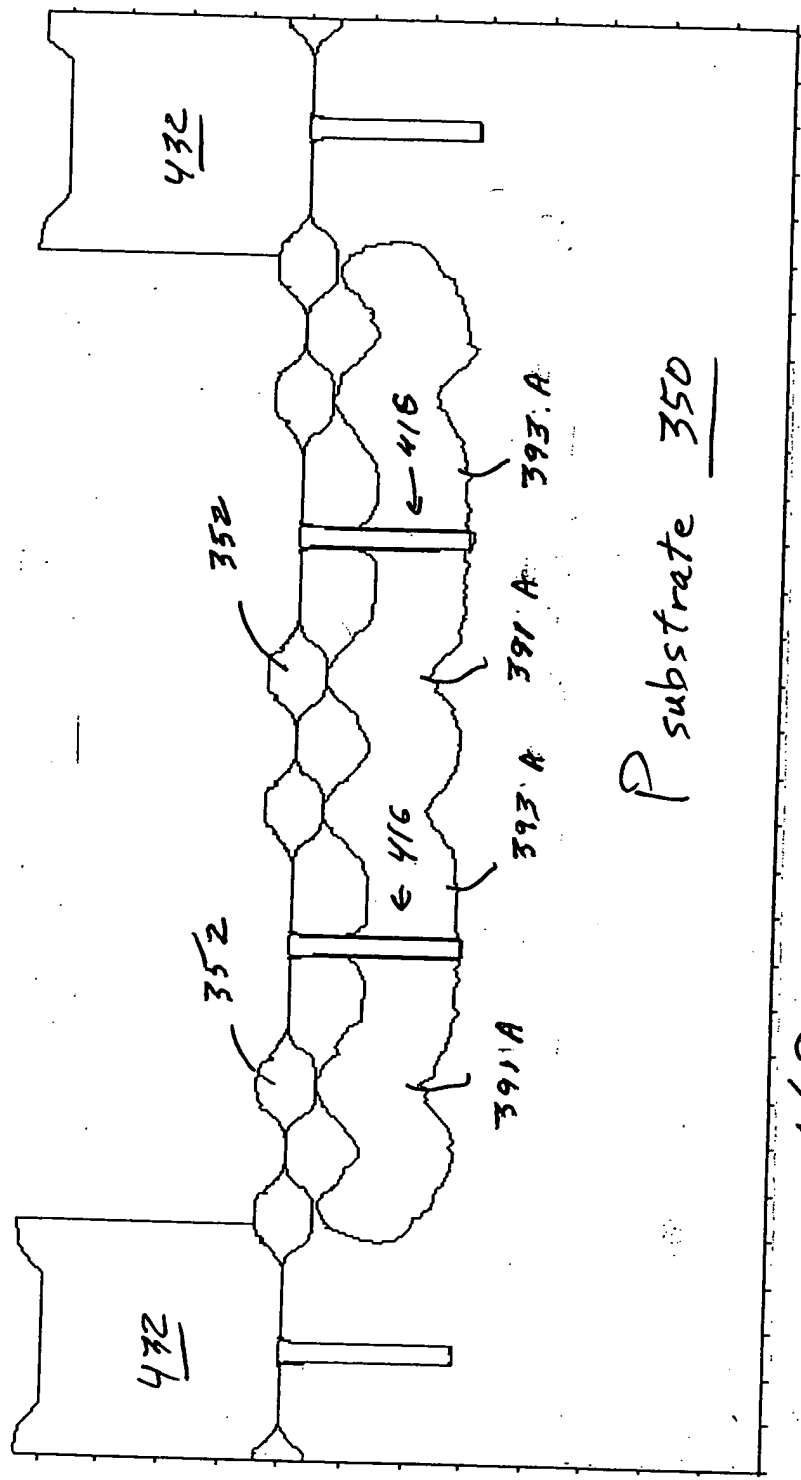
12V PMOS 309      12V NMOS 310



Deep N Mask and Implant  
Fig. 35E

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30 V Lateral Trench DMOS 308



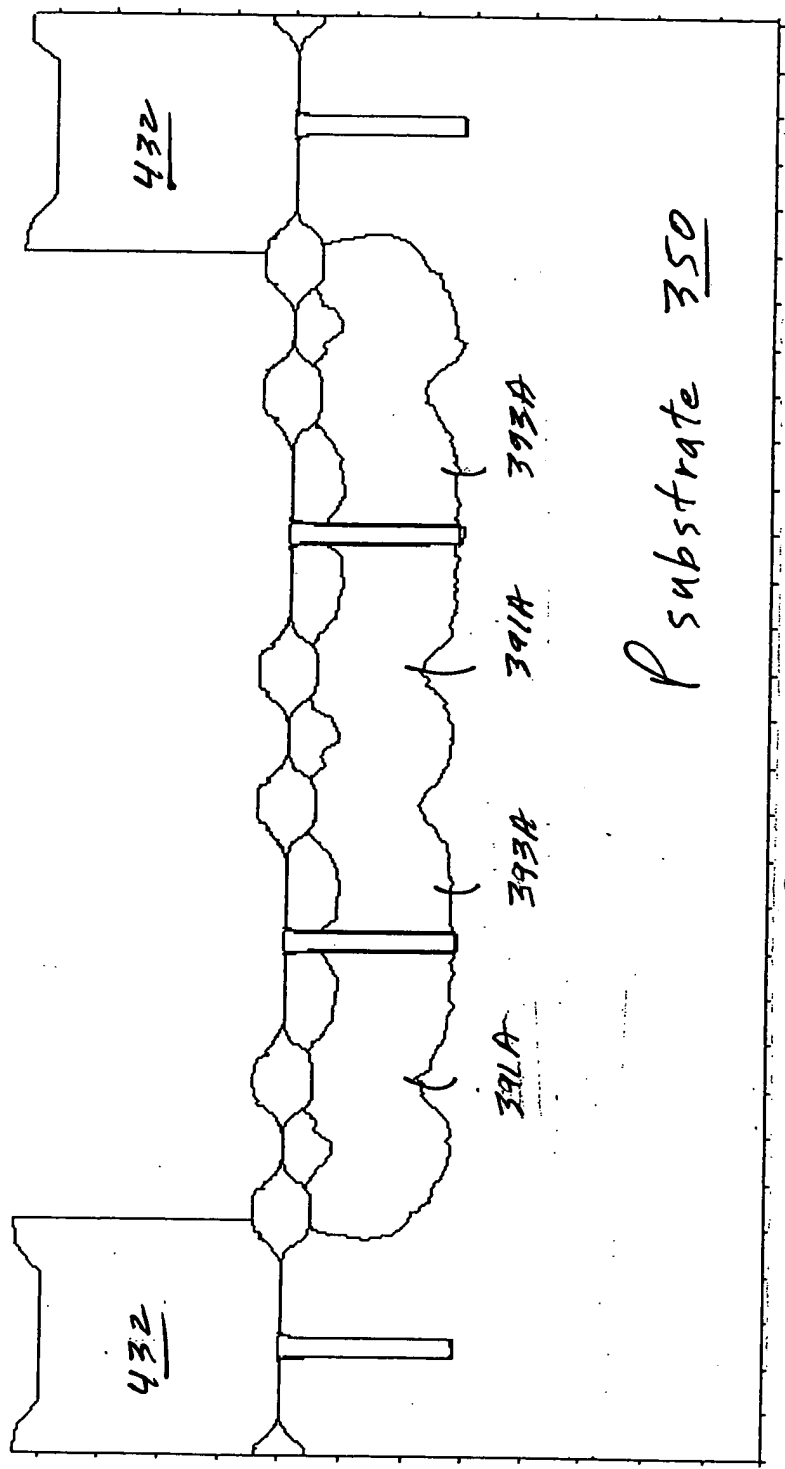
P substrate 350

N Drift Implant - First Stage

Fig. 36D

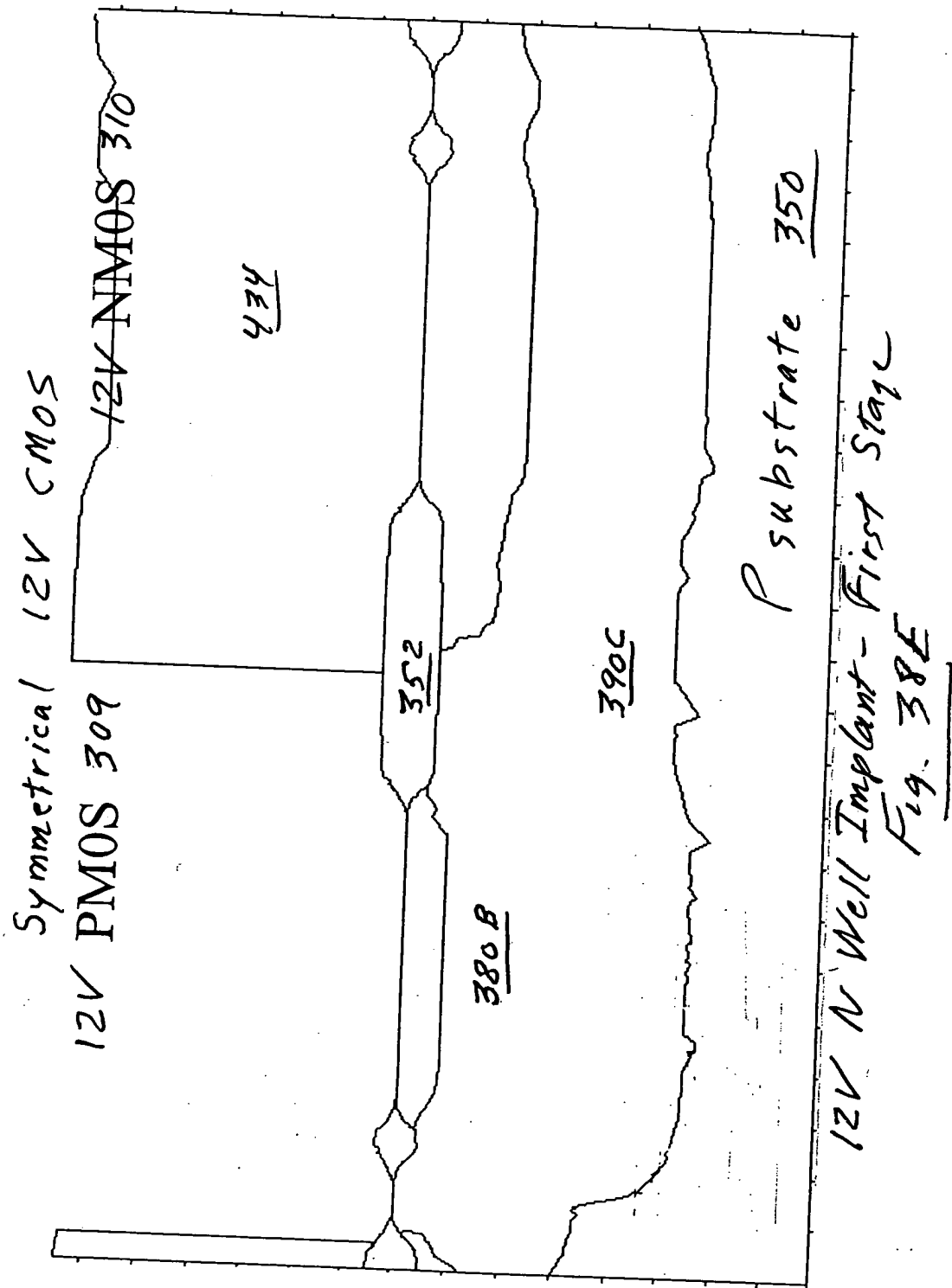
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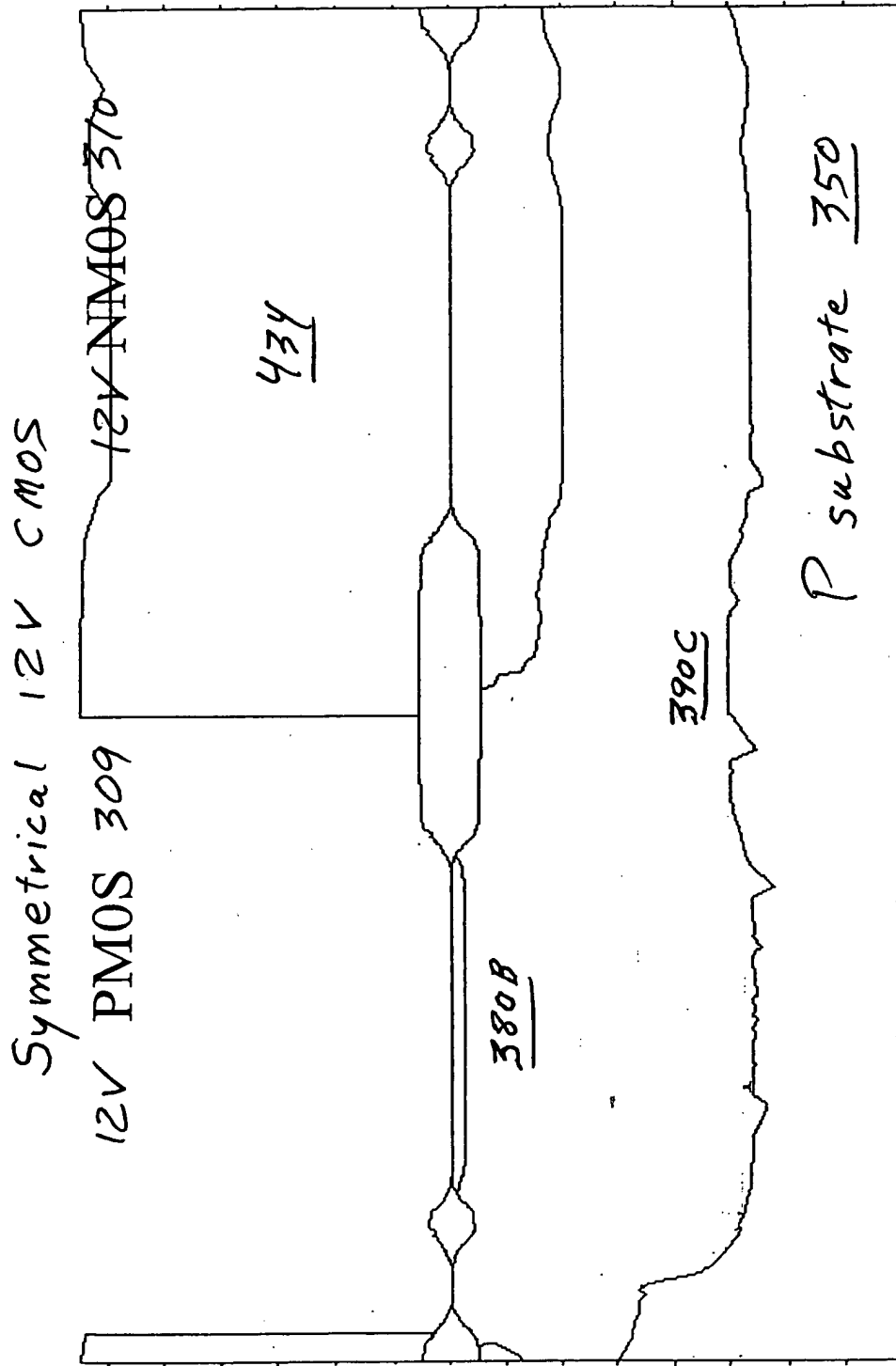
30V Lateral Trench DMOS 308



N Drift Implant - Second Stage  
Fig. 37D

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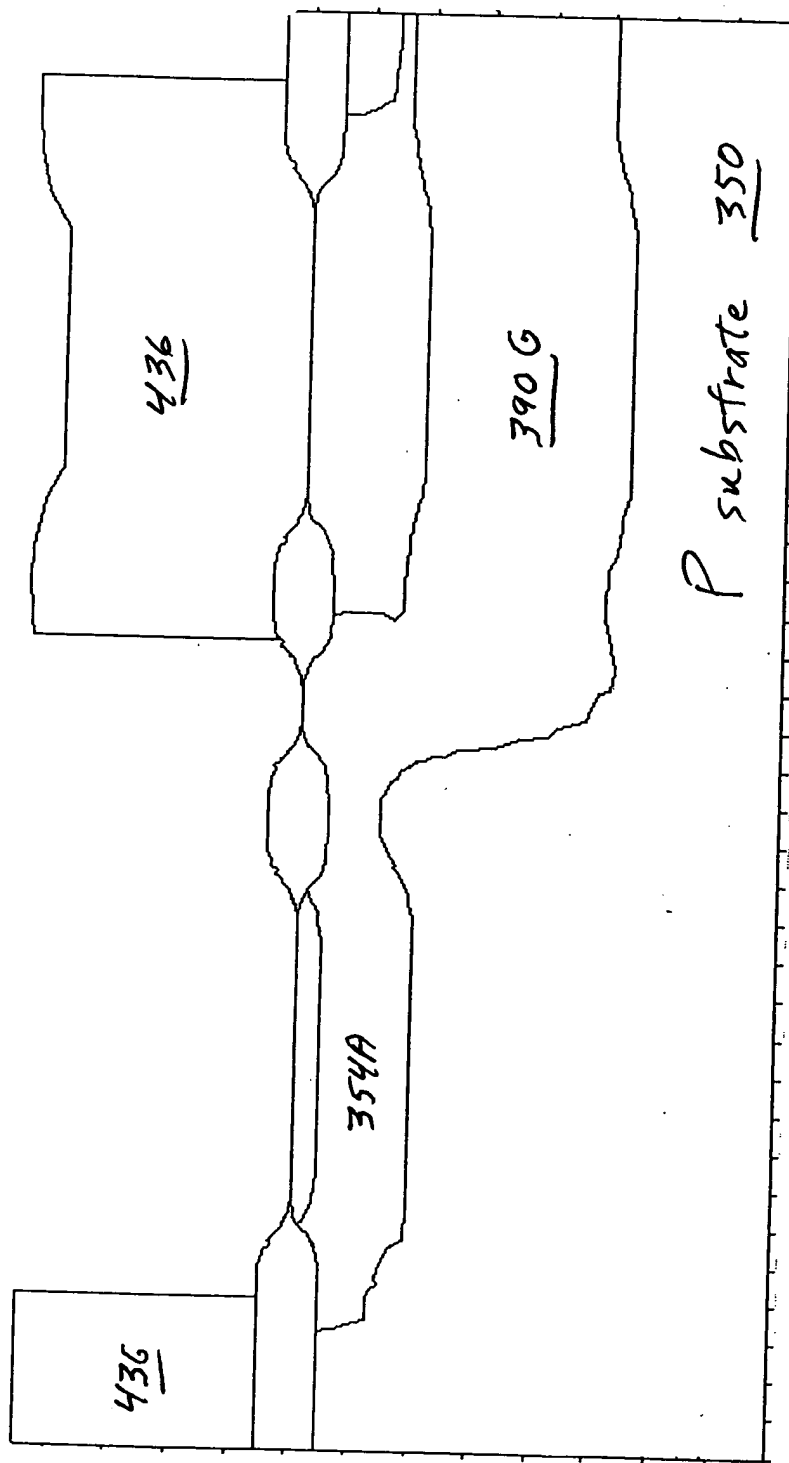


12V N Well Implant - Second Stage  
Fig. 39E



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5V PMOS 301      5V NMOS 302



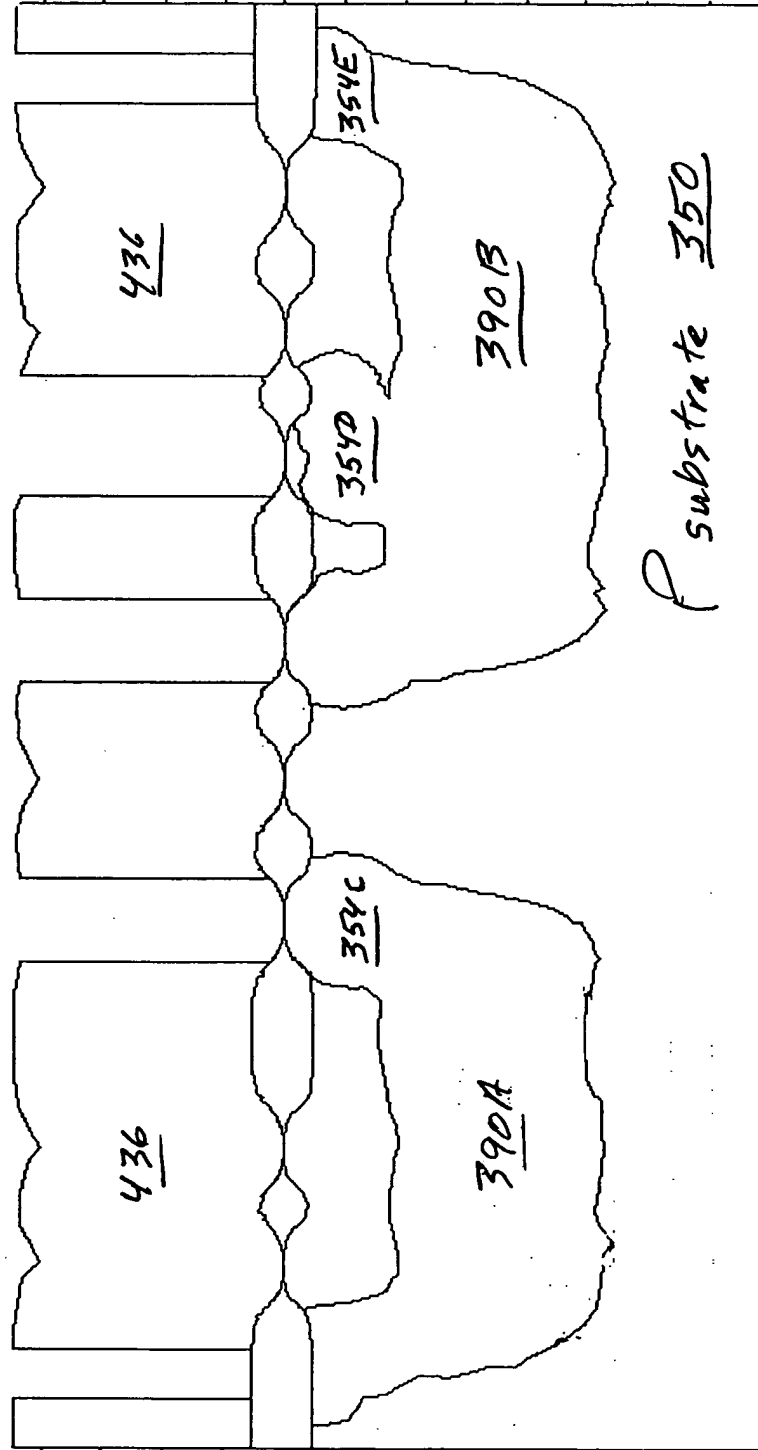
5V N Well Implant - First Stage

Fig. 40A

High F<sub>T</sub> Layout

5V NPN 305

5V PNP 306



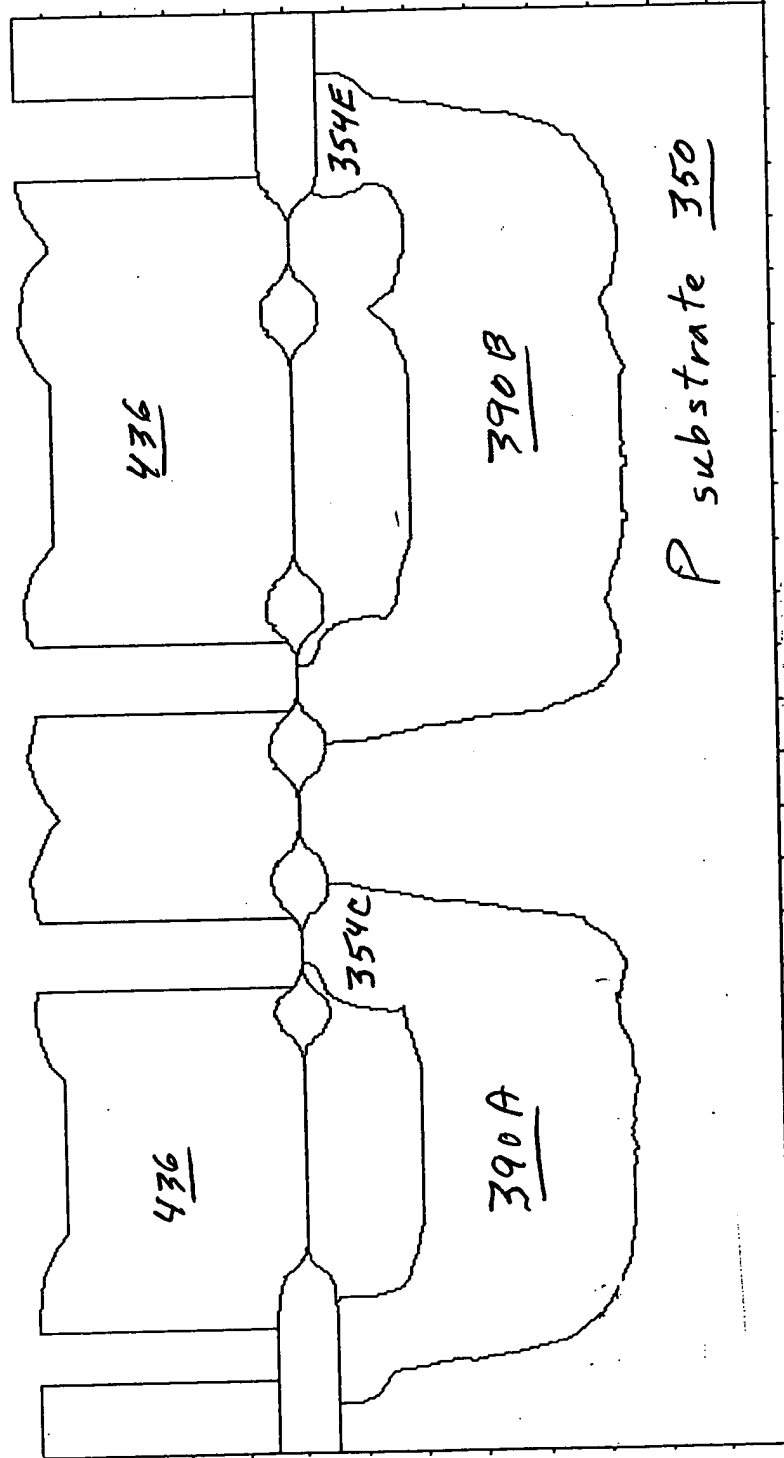
5V N Well Implant - First Stage

Fig. 40B

Conventional Layout

5V PNP

5V NPN

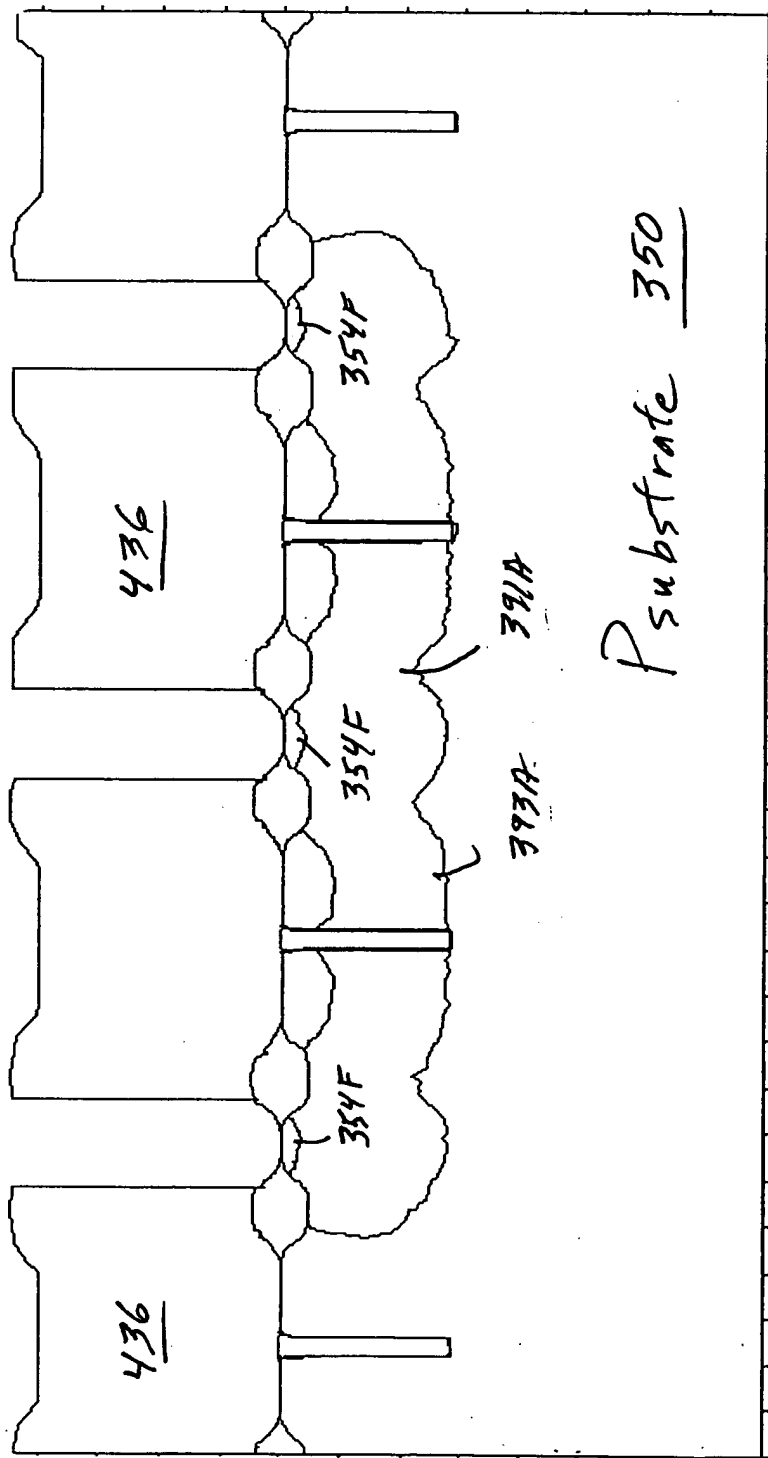


5V N Well Implant - First Stage

Fig. 40C

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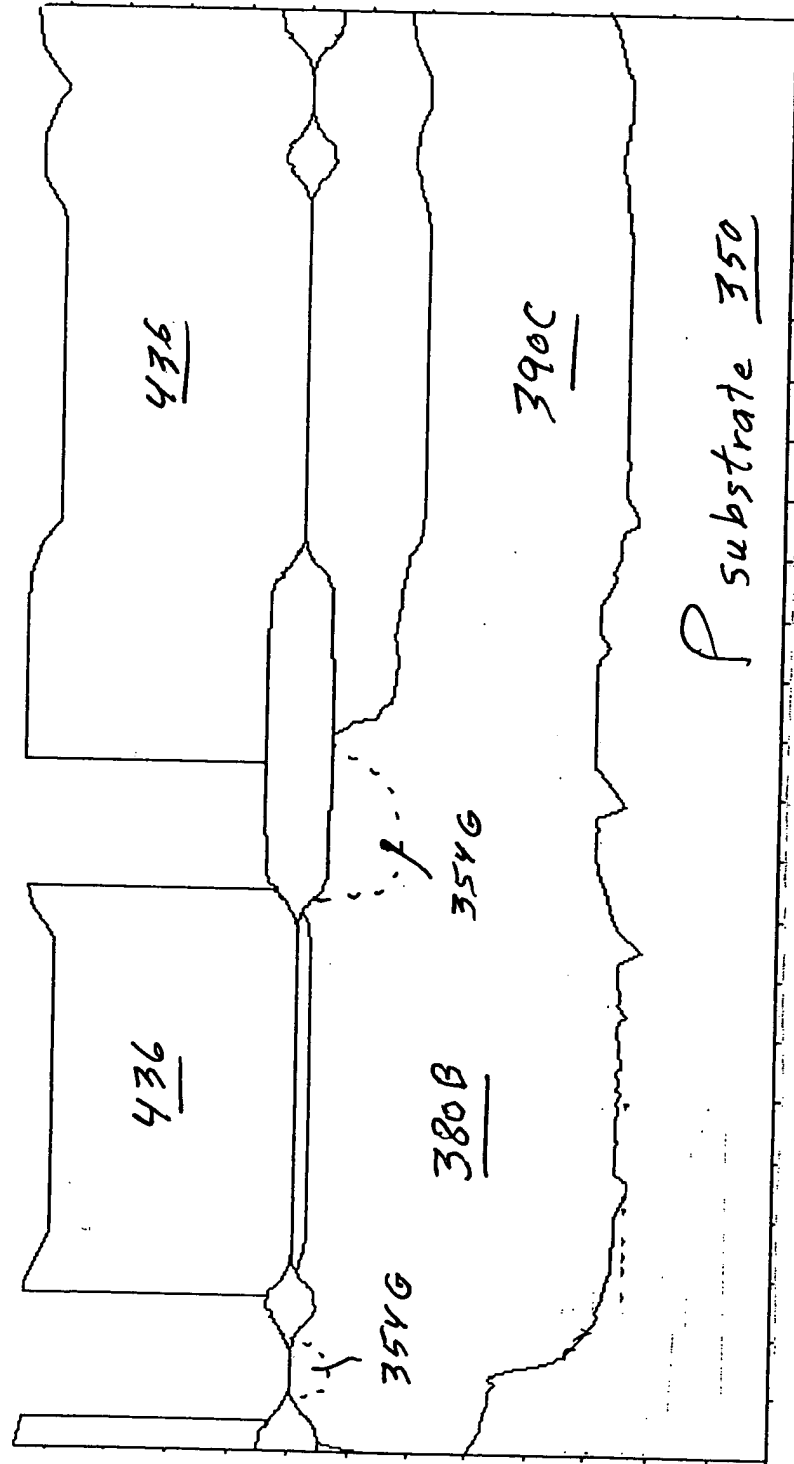
30V Lateral Trench DMOS 308



5V N Well Implant - First Stage

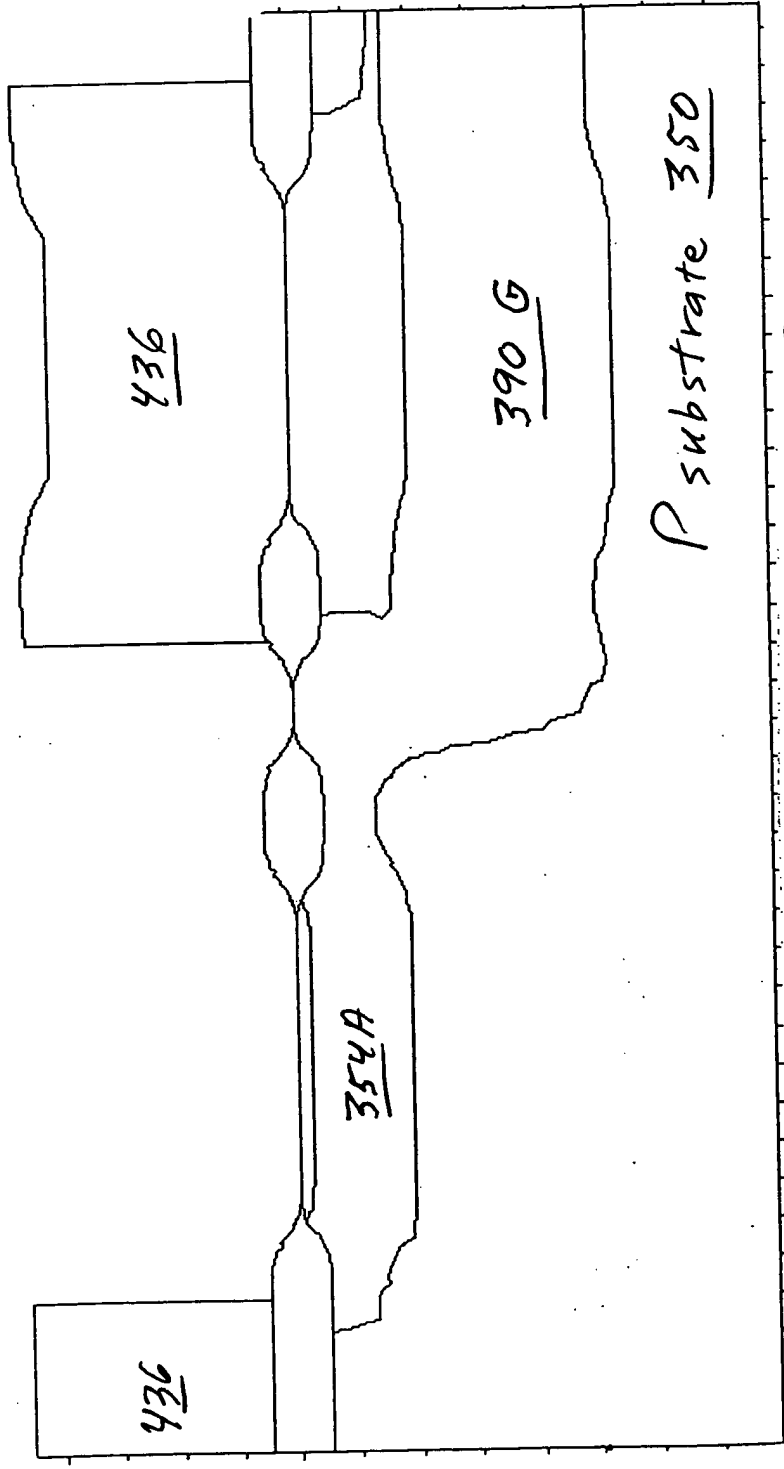
Fig 40D

Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



5V N Well Implant - First Stage  
Fig 40E

5V PMOS 301      5V NMOS 302

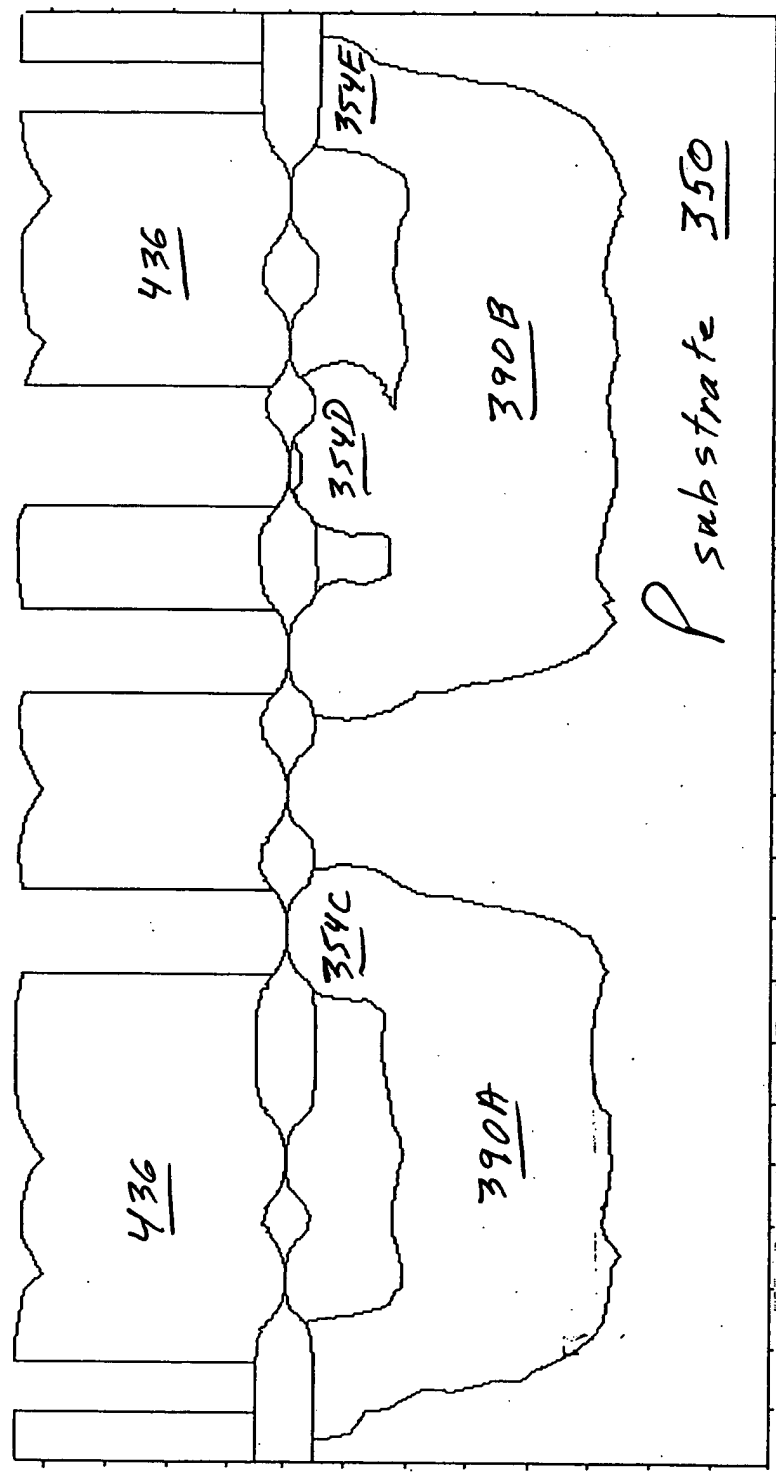


5V NWell Implant - Second Stage  
Fig. 41A

High  $F_T$  Layout

5V NPN 305

5V PNP 306



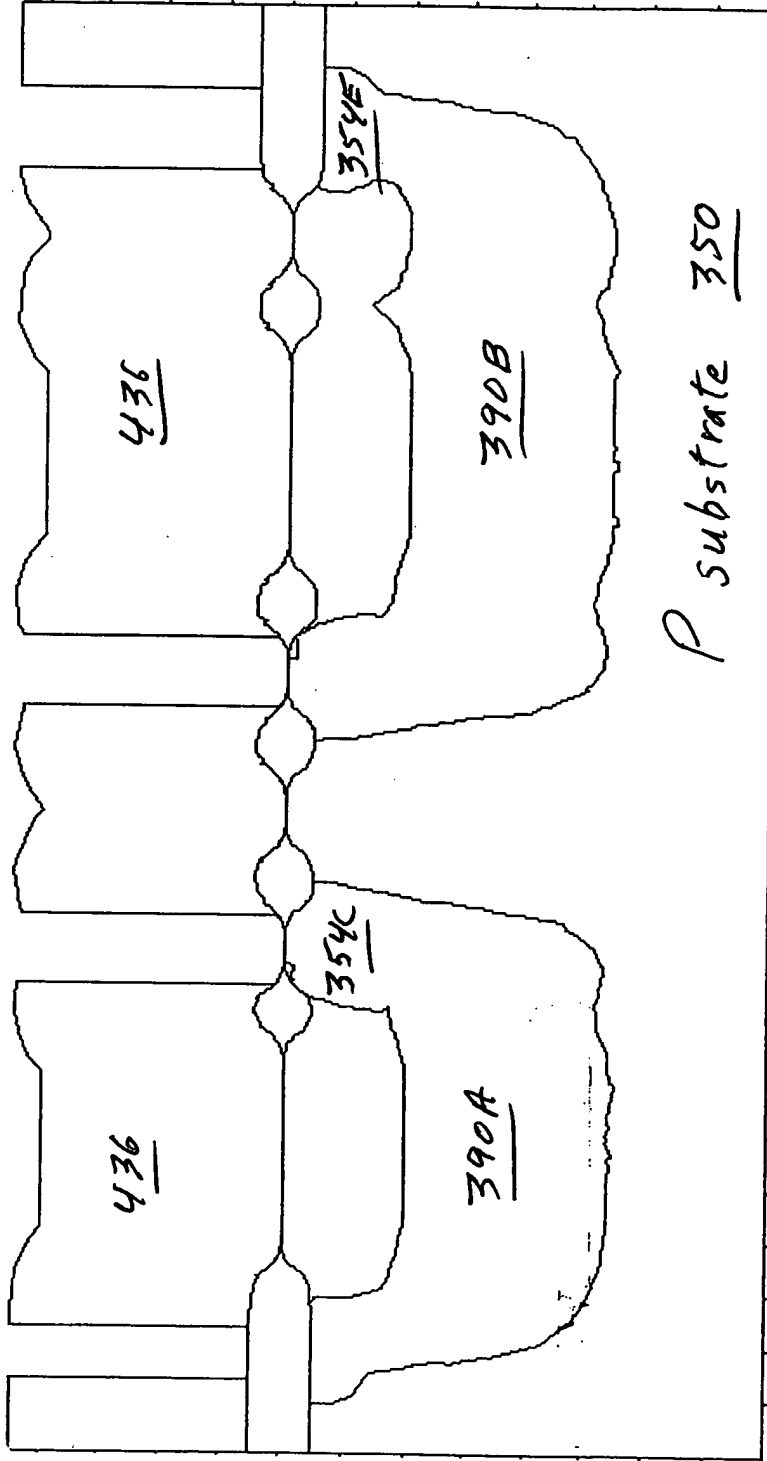
5V N Well Implant - Second Stage

Fig. 41B

Conventional Layout

5V NPN

5V PNP

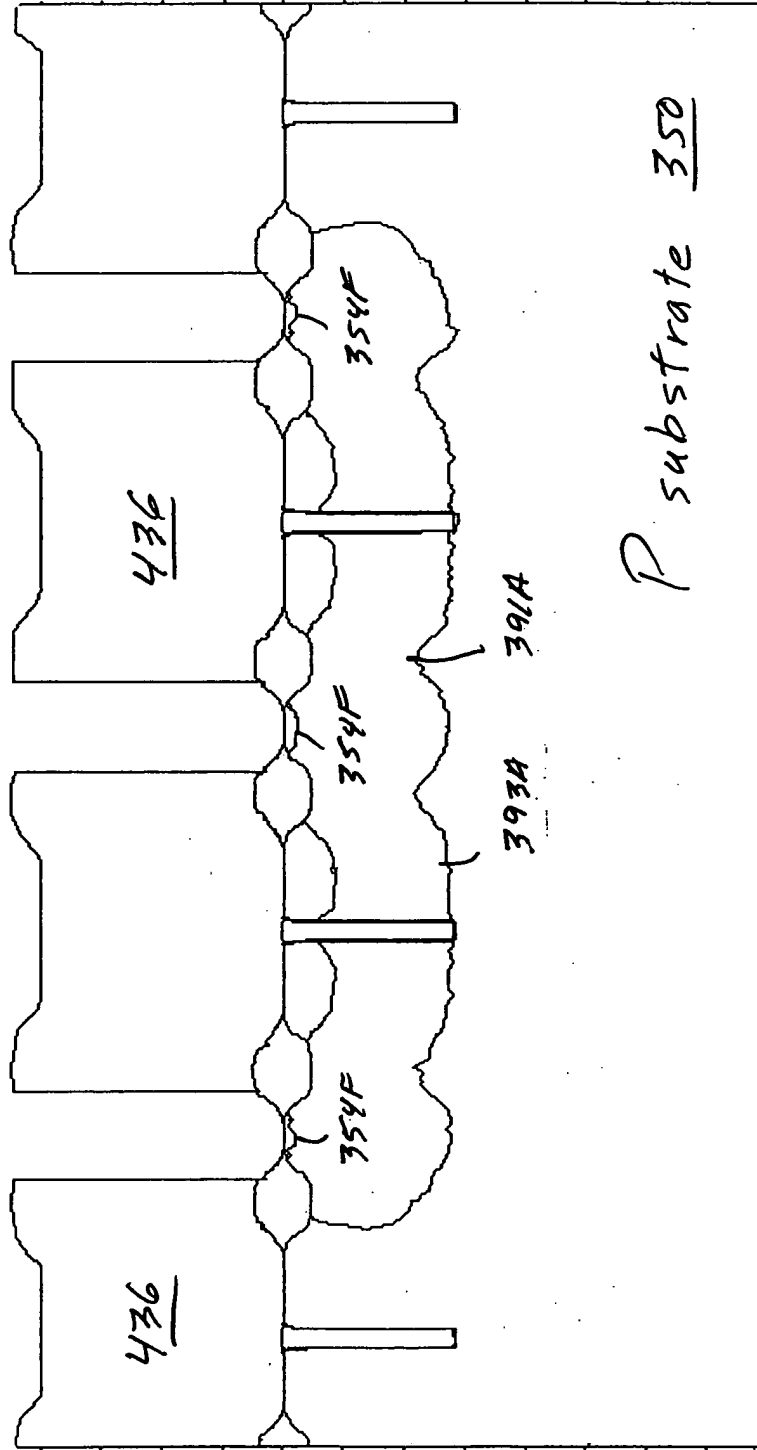


5V N Well Implant - Second Stage

Fig. 41C



30V Lateral Trench DMOS 308

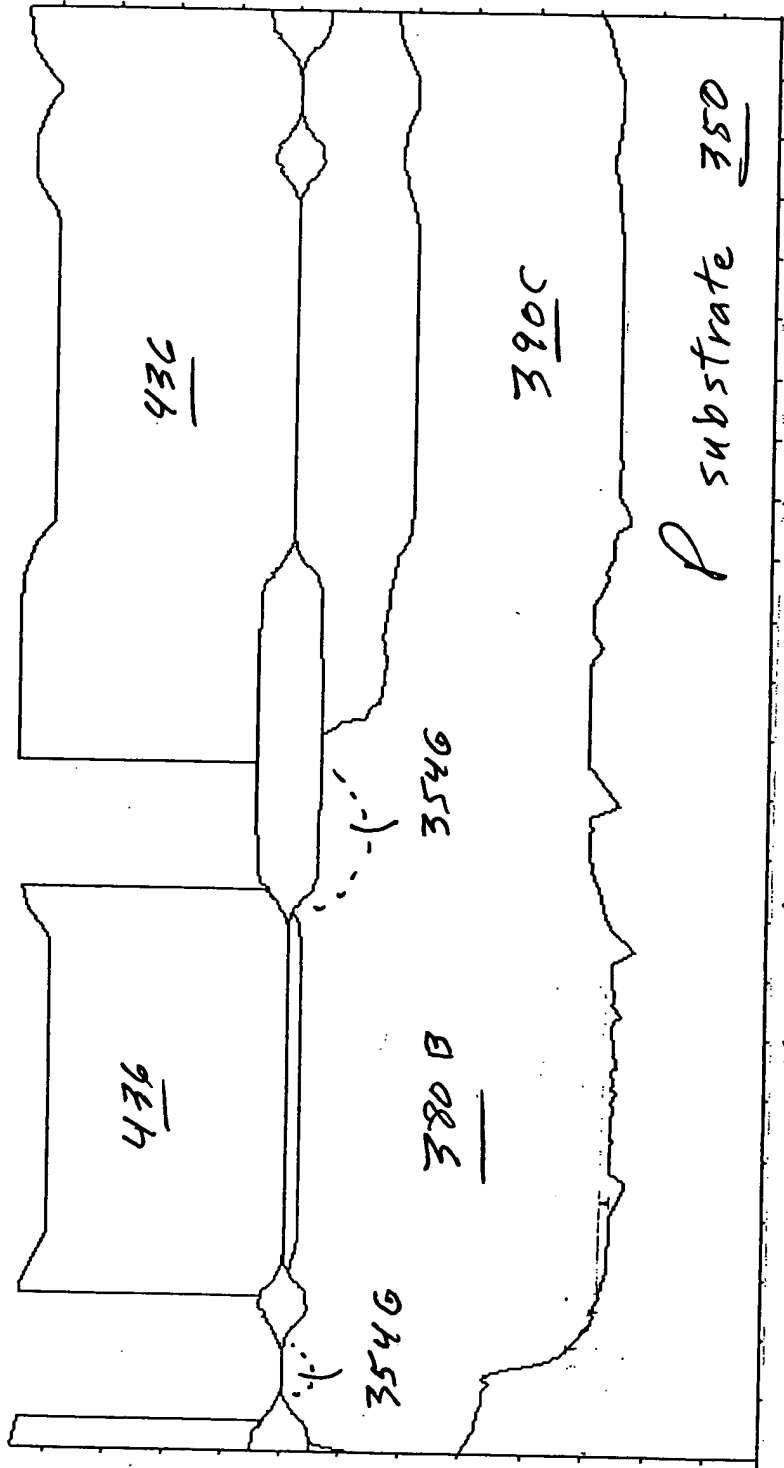


P substrate 350

5V NWell Implant - Second Stage

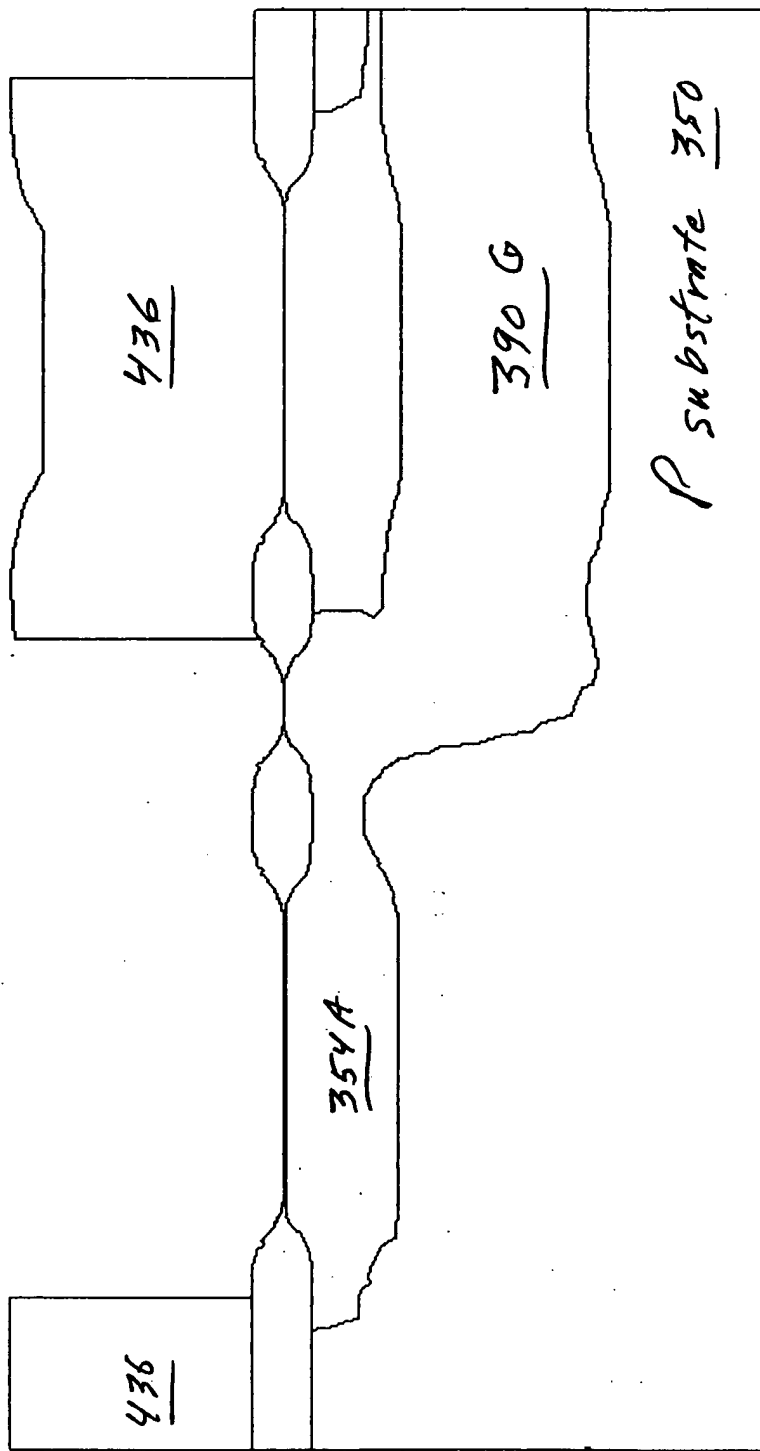
Fig. 41D

Symmetrical 12V CMOS  
 12V PMOS 309 12V NMOS 310



5V NWell Implant - Second Stage  
Fig. 41E

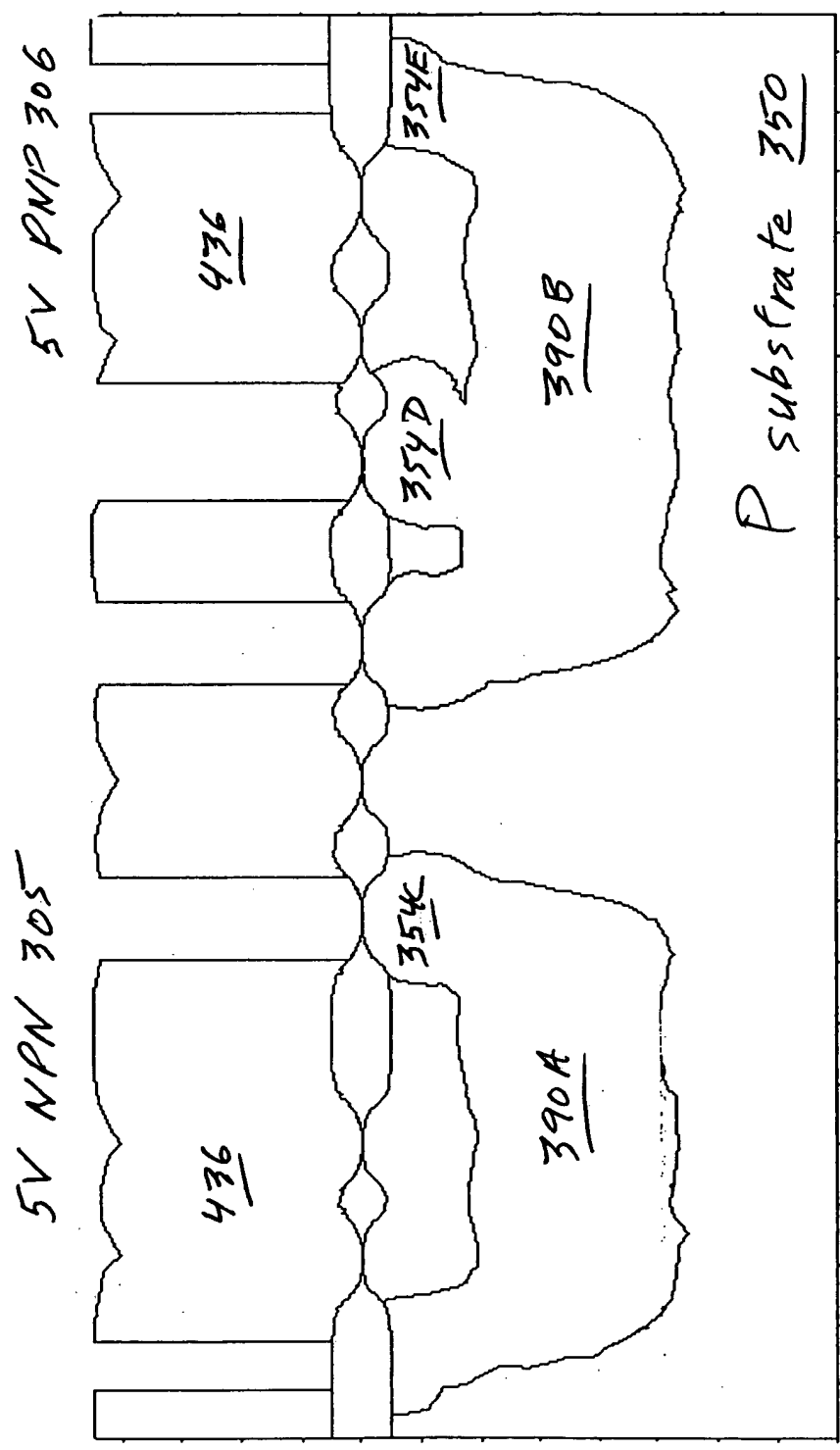
5V PMOS 301      5V NMOS 302



5V N Well Implant - Third Stage

Fig. 42A

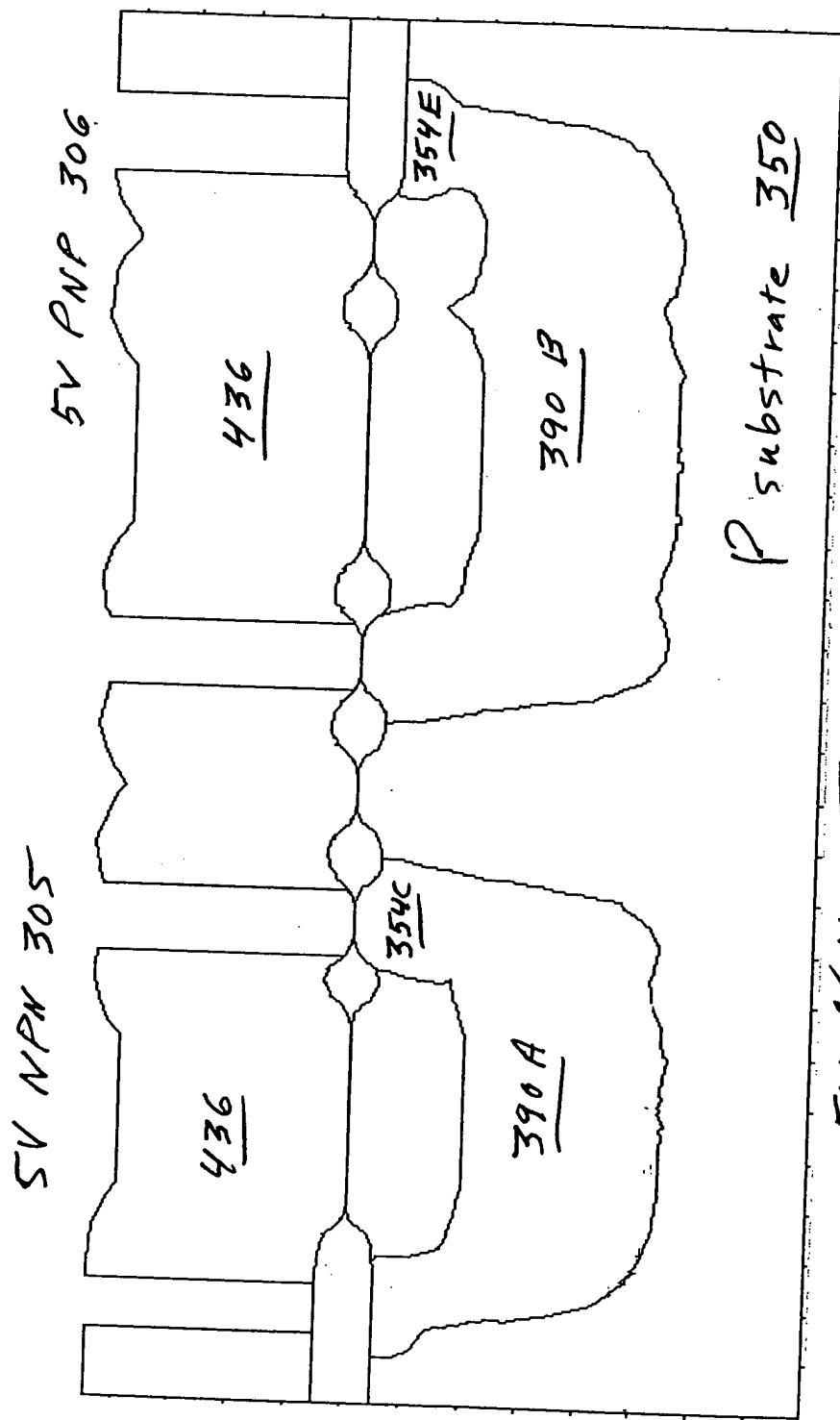
High F<sub>T</sub> Layout



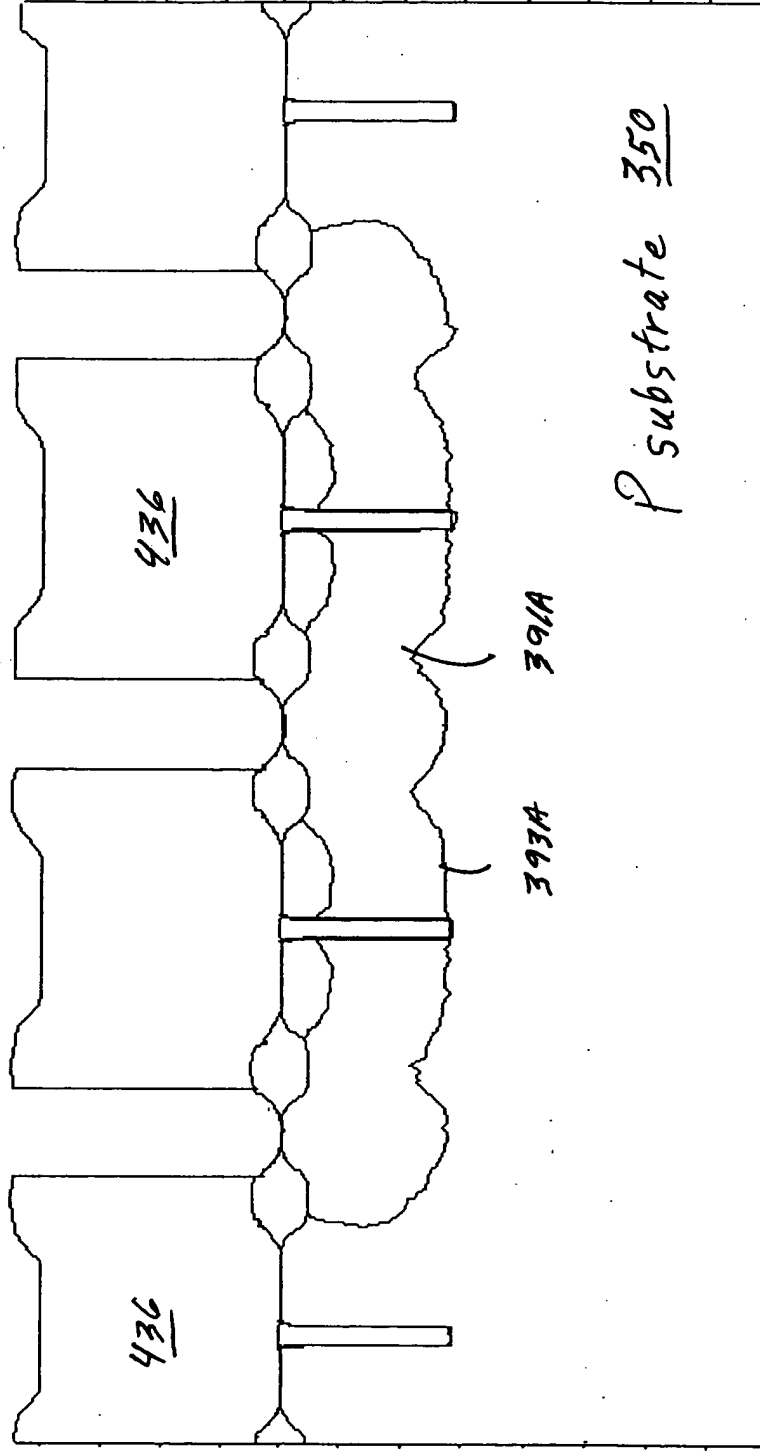
5V NWell Implant - Third Stage

Fig. 42B

## Conventional Layout

5V N Well Implant - Third Stage  
Fig. 42C

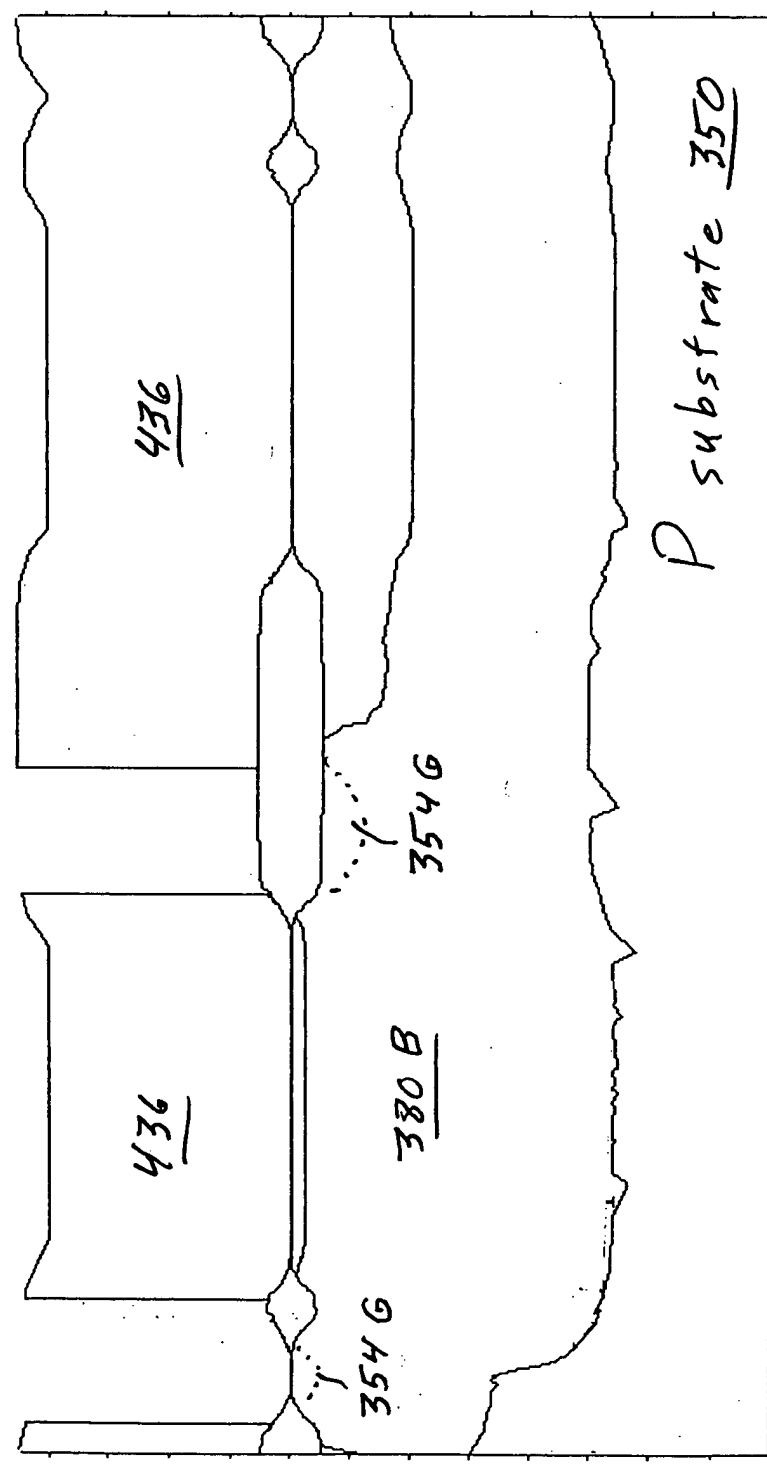
30V Lateral Trench DMOS 308



5V N Well Implant - Third Stage

Fig. 42D

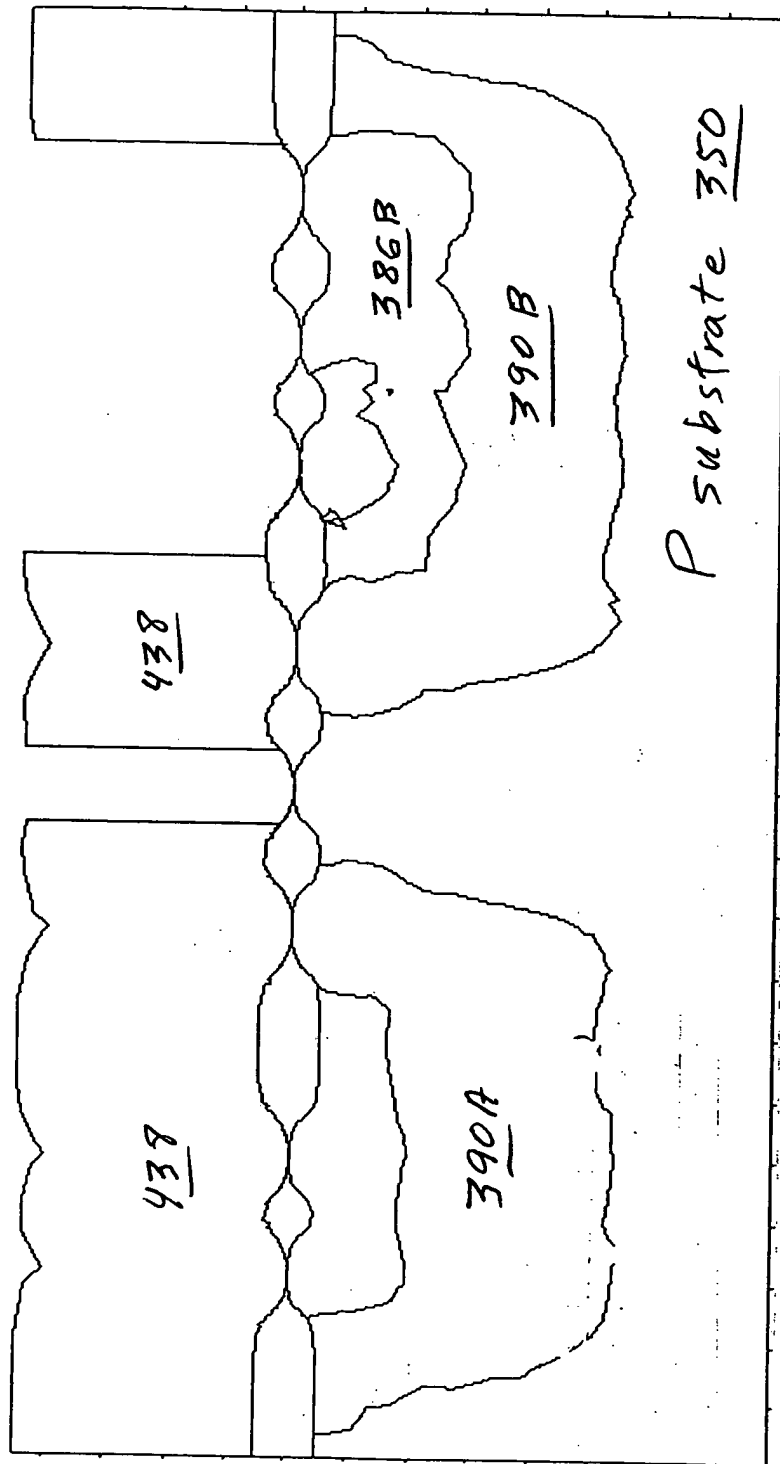
Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



5V N Well Implant - Third Stage  
Fig. 42E

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High Fr Layout  
5V NPN 305      5V PNP 306



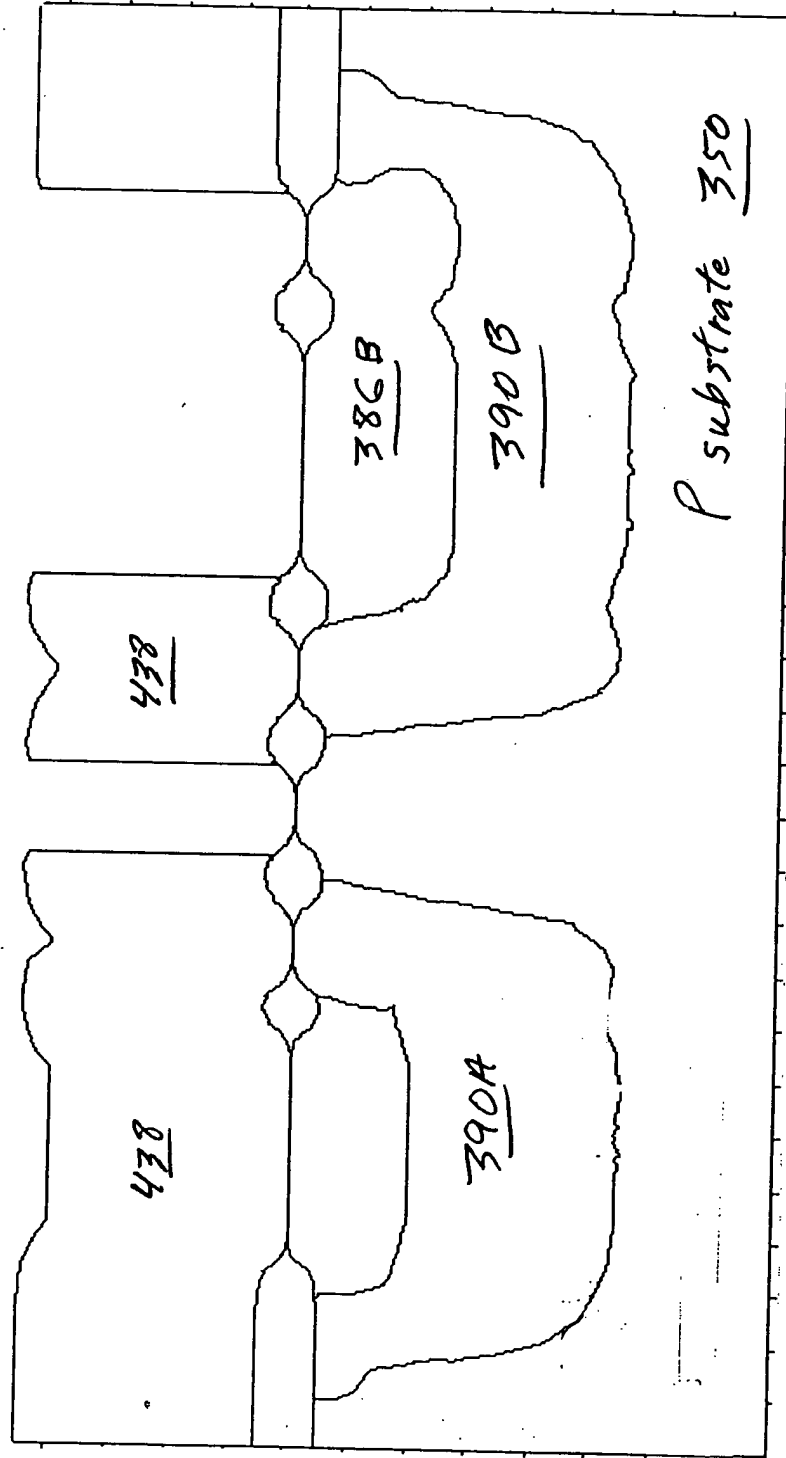
12V P Well Implant - First Stage  
Fig. 43B



Conventional Layout

5V NPN

5V PNP

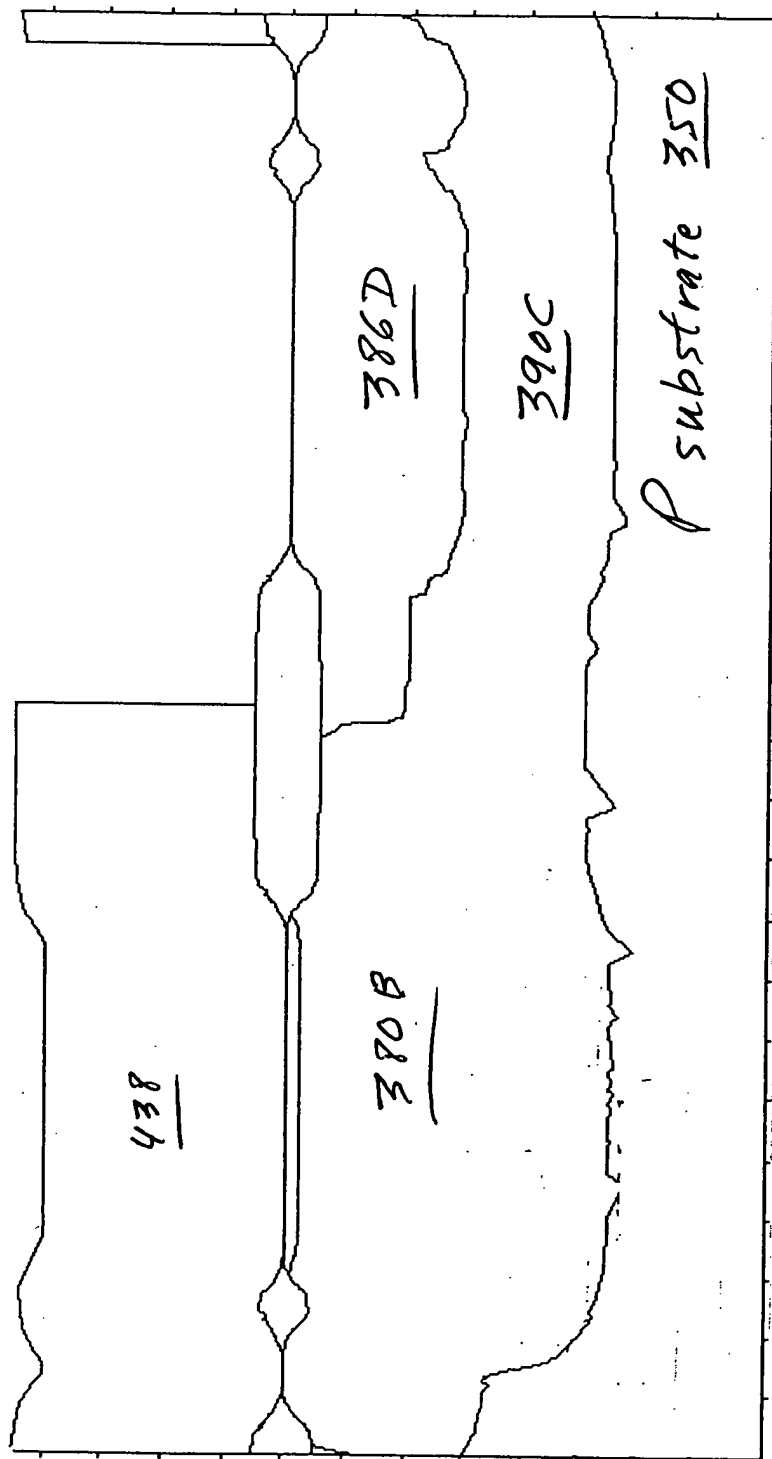


12V P Well Implant - First Stage

Fig. 43C

Symmetrical 12V CMOS

12V	✓	PMOS	309	12V	NMOS	310
-----	---	------	-----	-----	------	-----

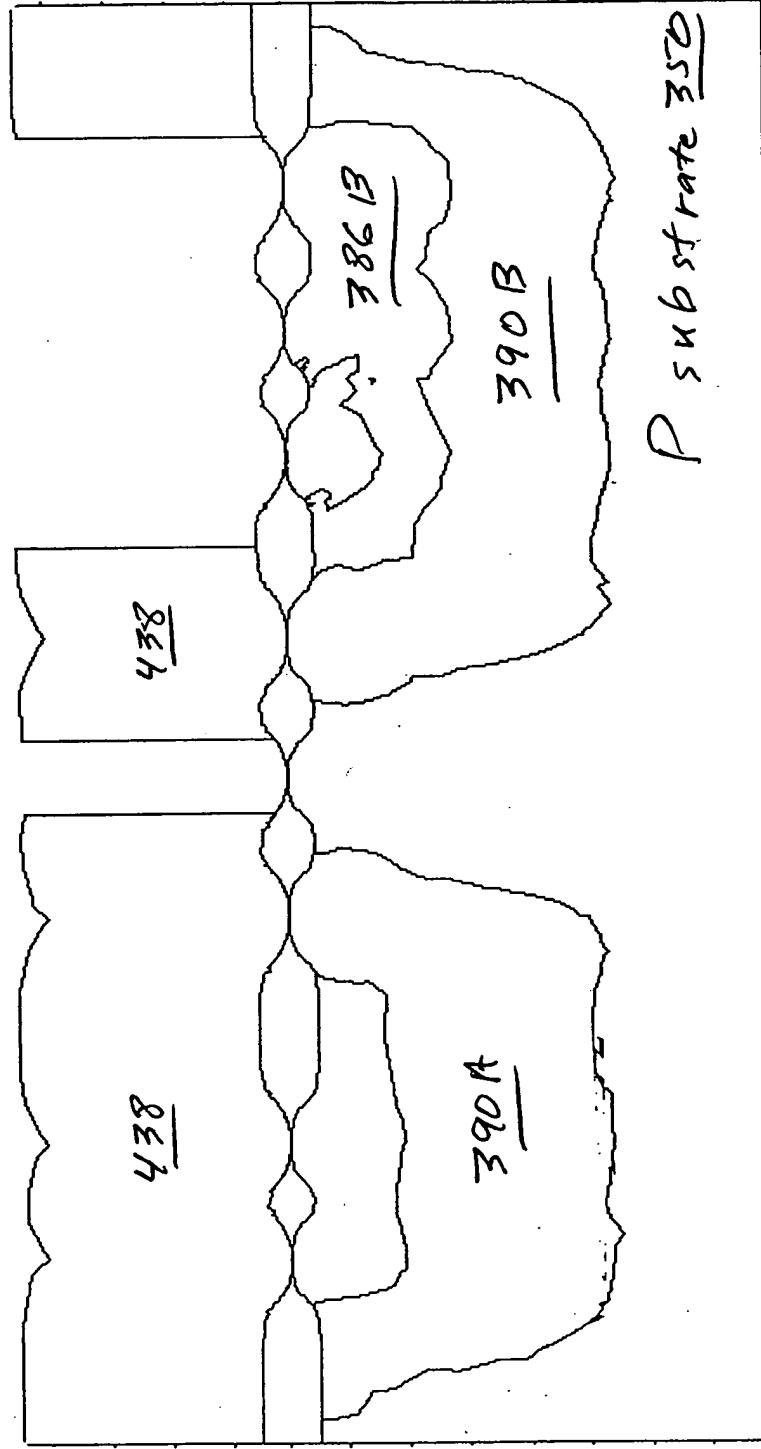


12V PiWell Implant - First Stage  
Fig 43E

# High F<sub>T</sub> Layout

5V NPN 305

5V PNP 306



12V P Well Implant - Second Stage

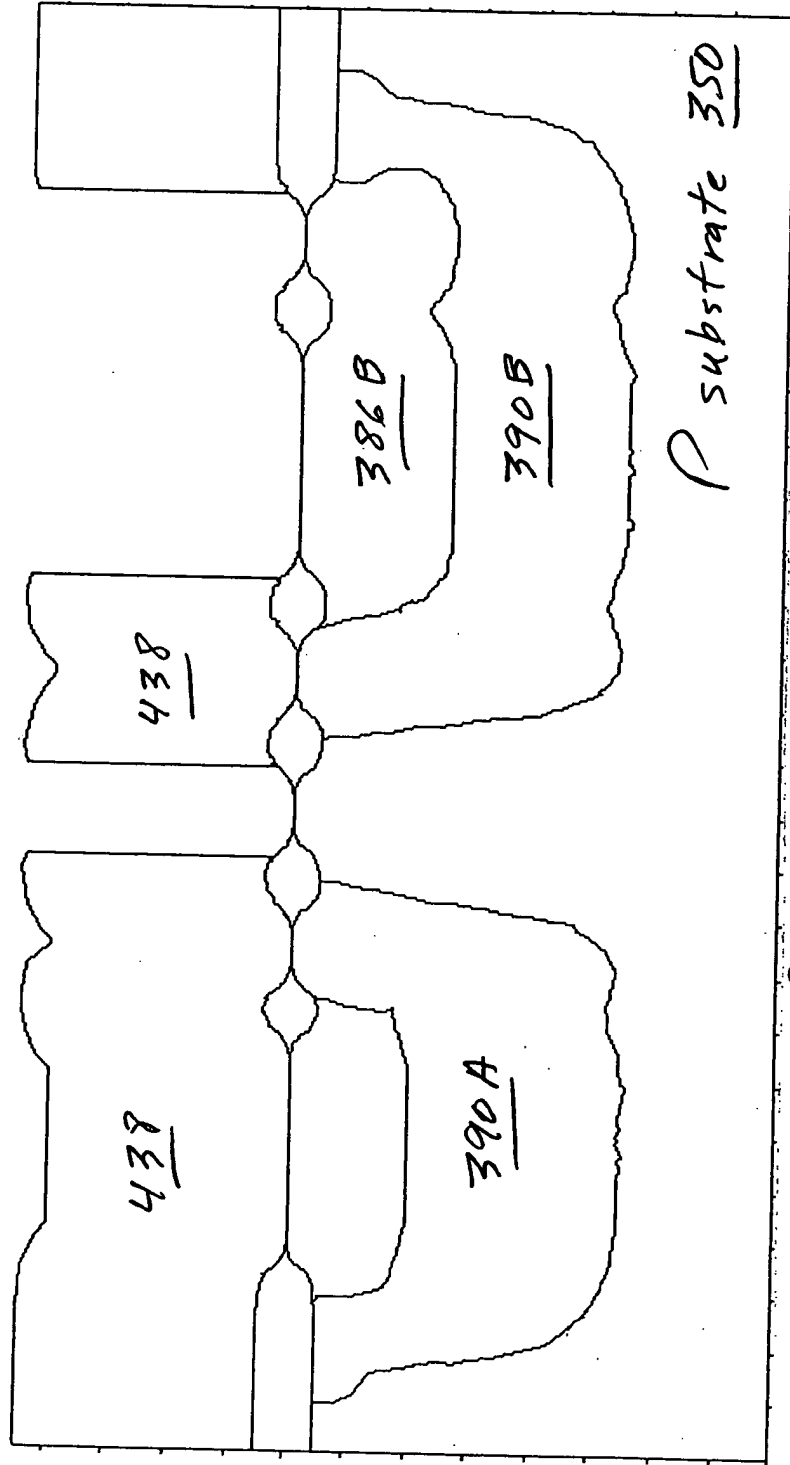
Fig. 44B

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Conventional Layout

5V NPN 305

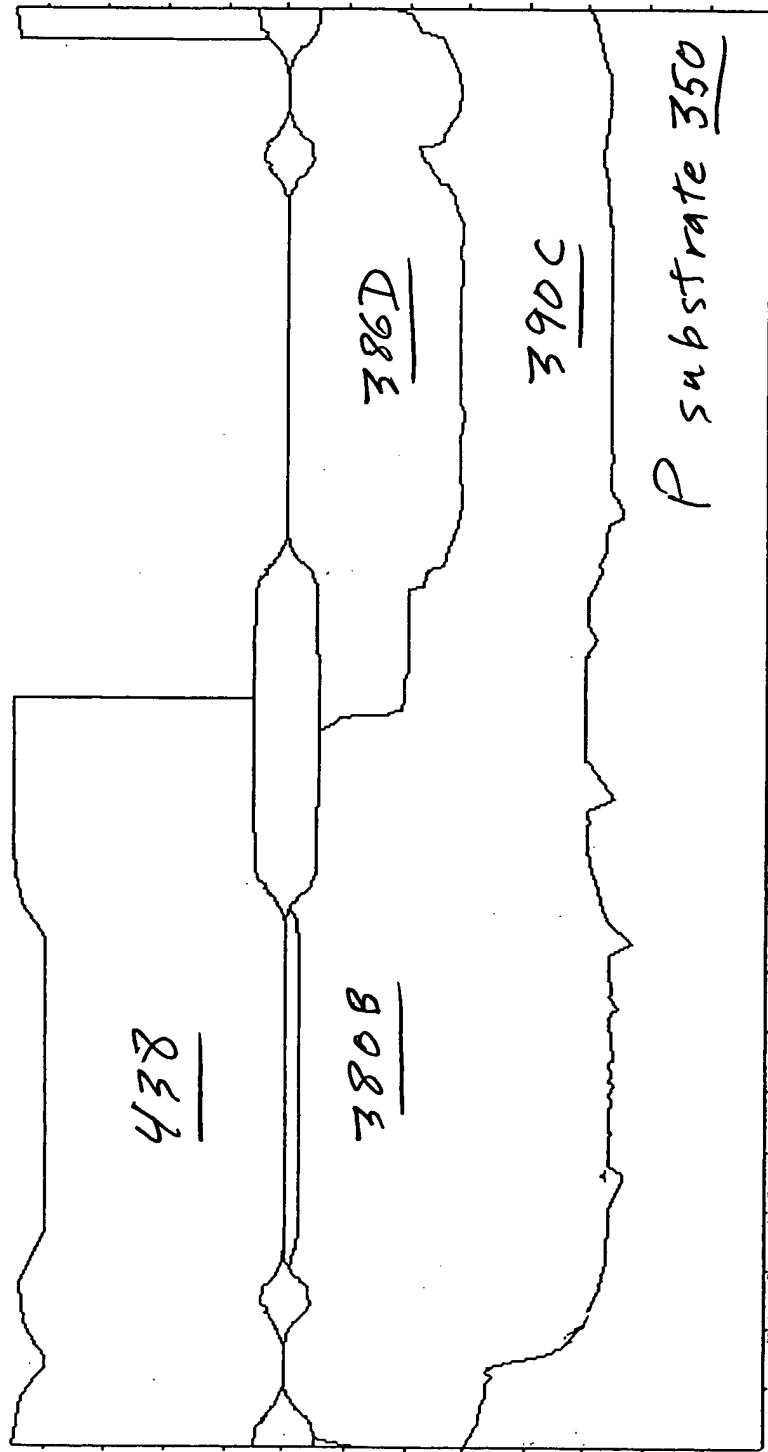
5V PNP 306



12V P Well Implant - Second Stage

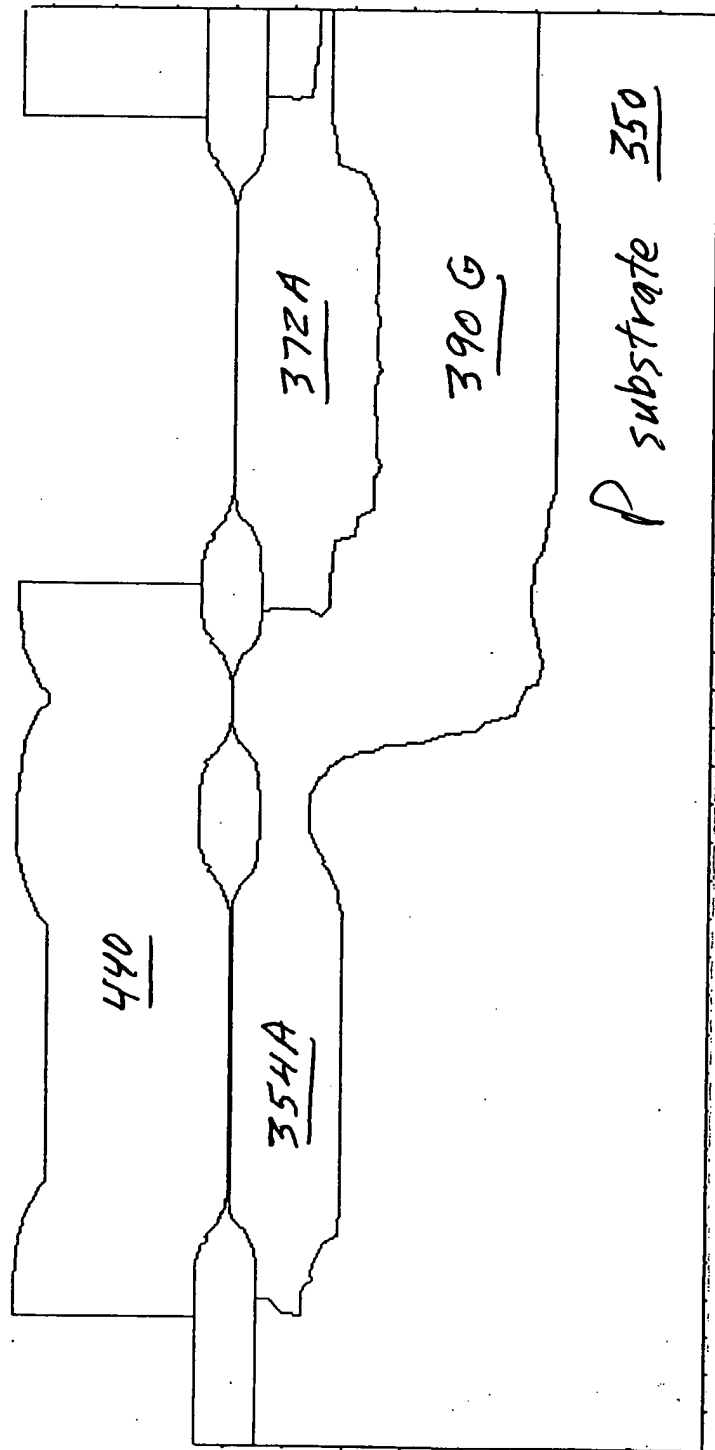
Fig 44C

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



12V P Well Implant - Second Stage  
Fig. 44E

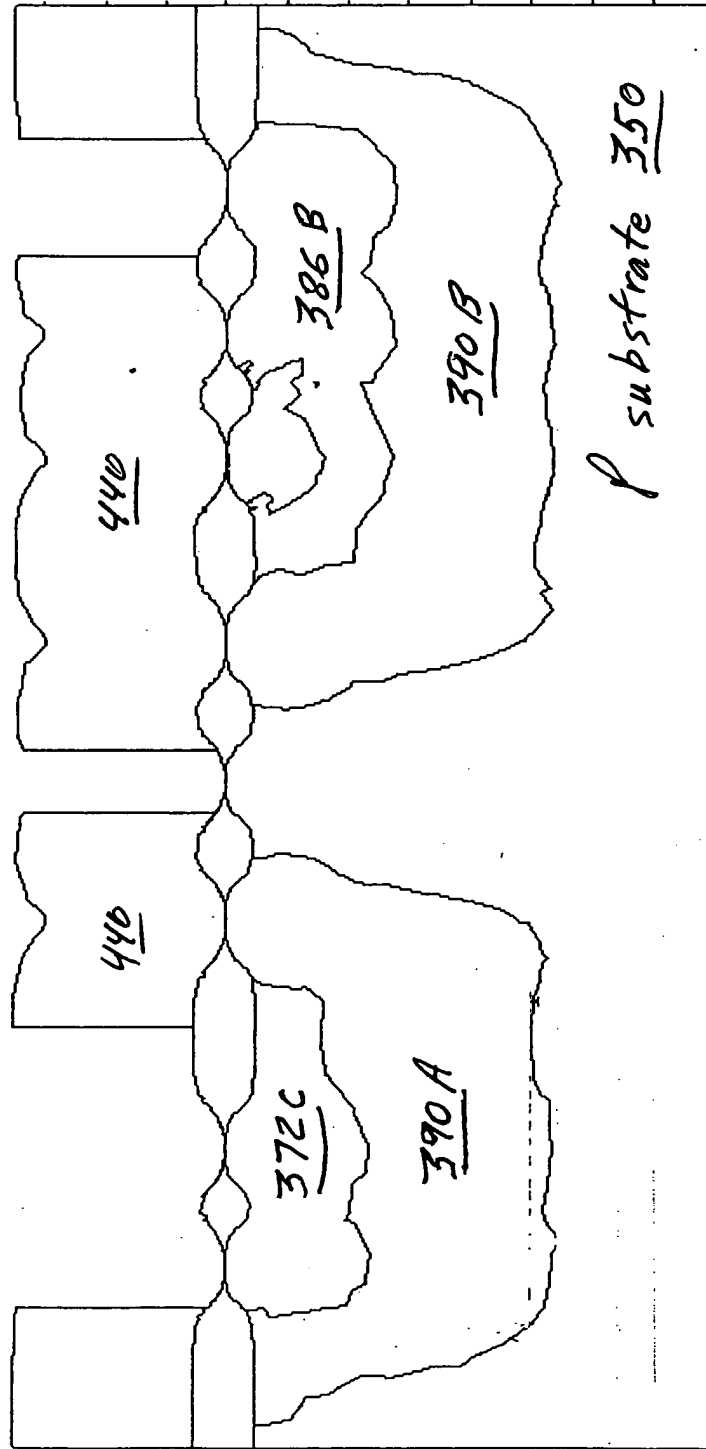
5V PMOS 301      5V NMOS 302



5V P Well Implant - First Stage  
Fig. 45A

High F<sub>T</sub> Layout

5V NPN 305      5V PNP 306



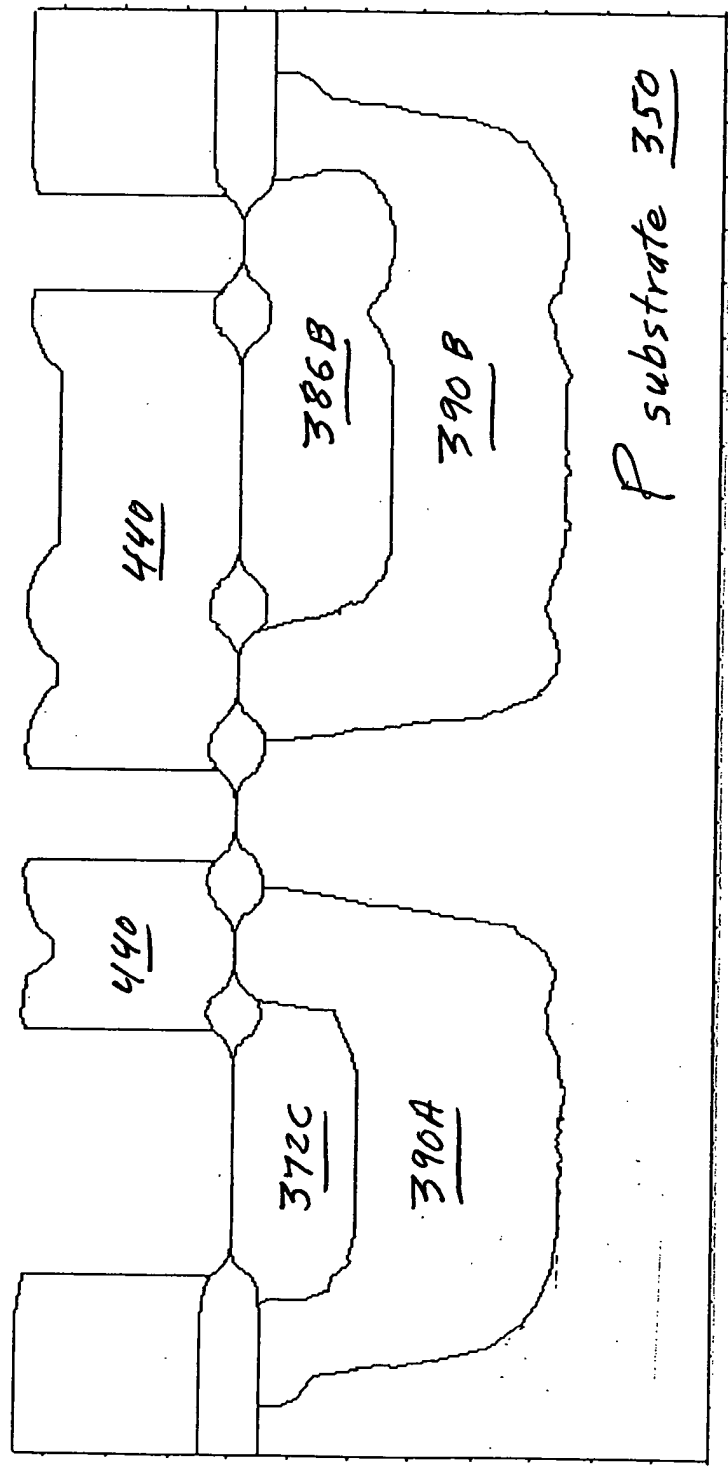
5V P Well Implant - First Stage

Fig. 45B

Conventional Layout

5V NPN

5V PNP

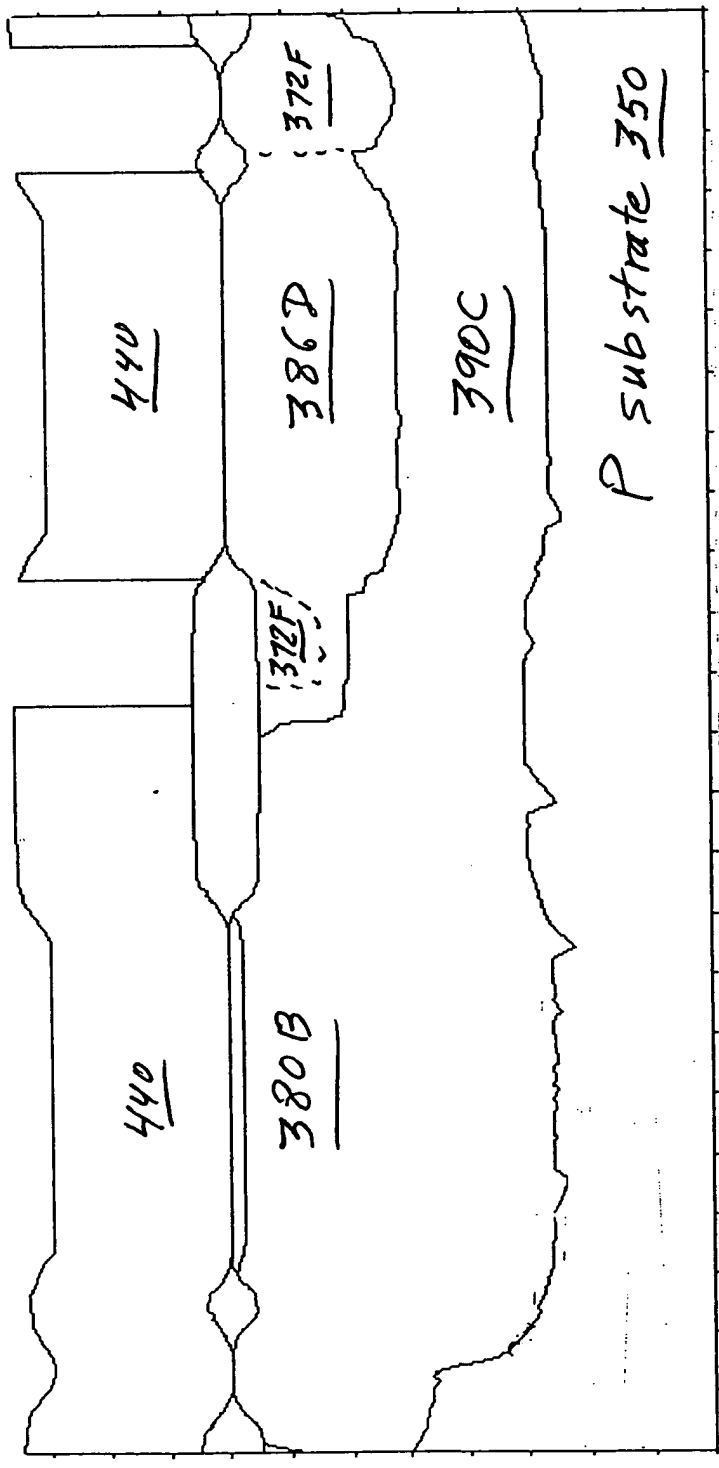


5V P Well Implant - First Stage

Fig. 45C

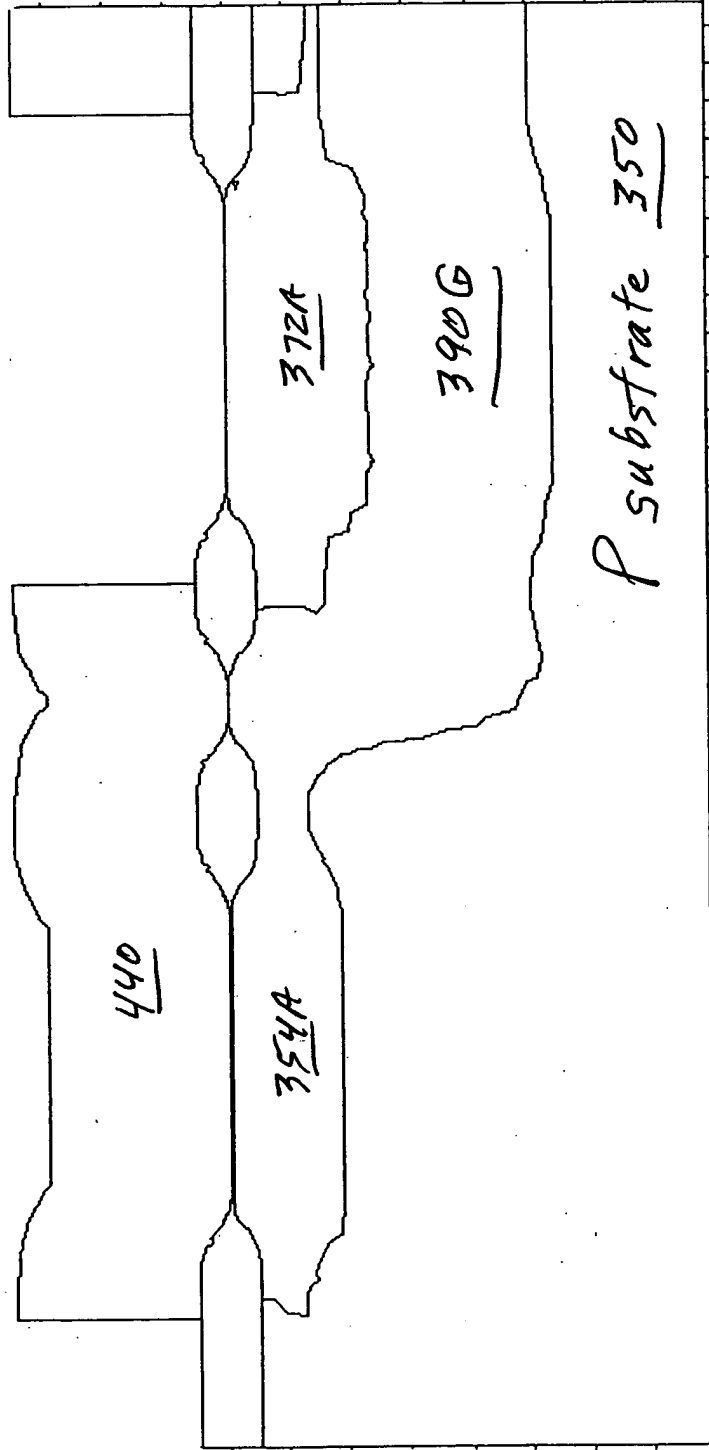


Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



5V P Well Implant - First Stage  
Fig. 45E

5V PMOS 301      5V NMOS 302

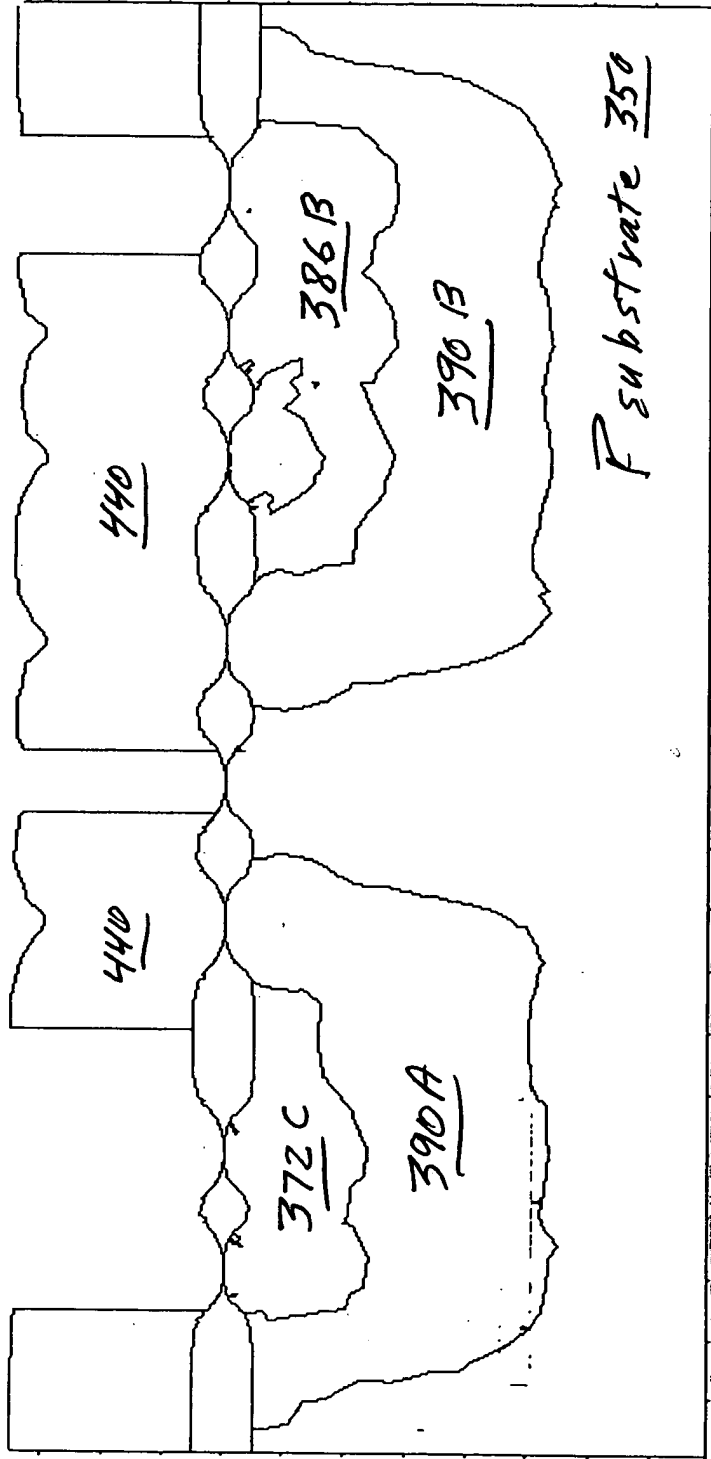


5V P Well Implant - Second Stage  
Fig 46A

High  $F_T$  Layout

5V NPN 305

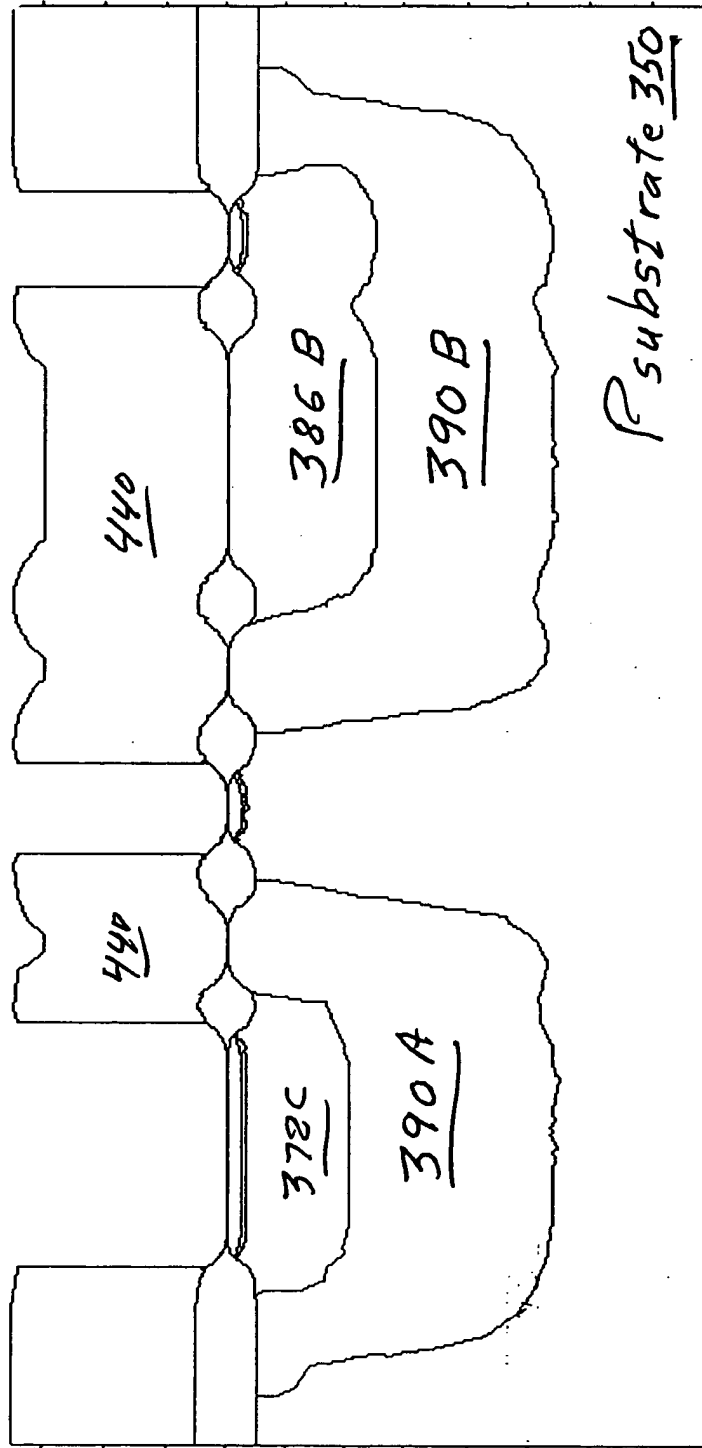
5V PNP 306



5V P Well Implant - Second Stage

Fig. 46B

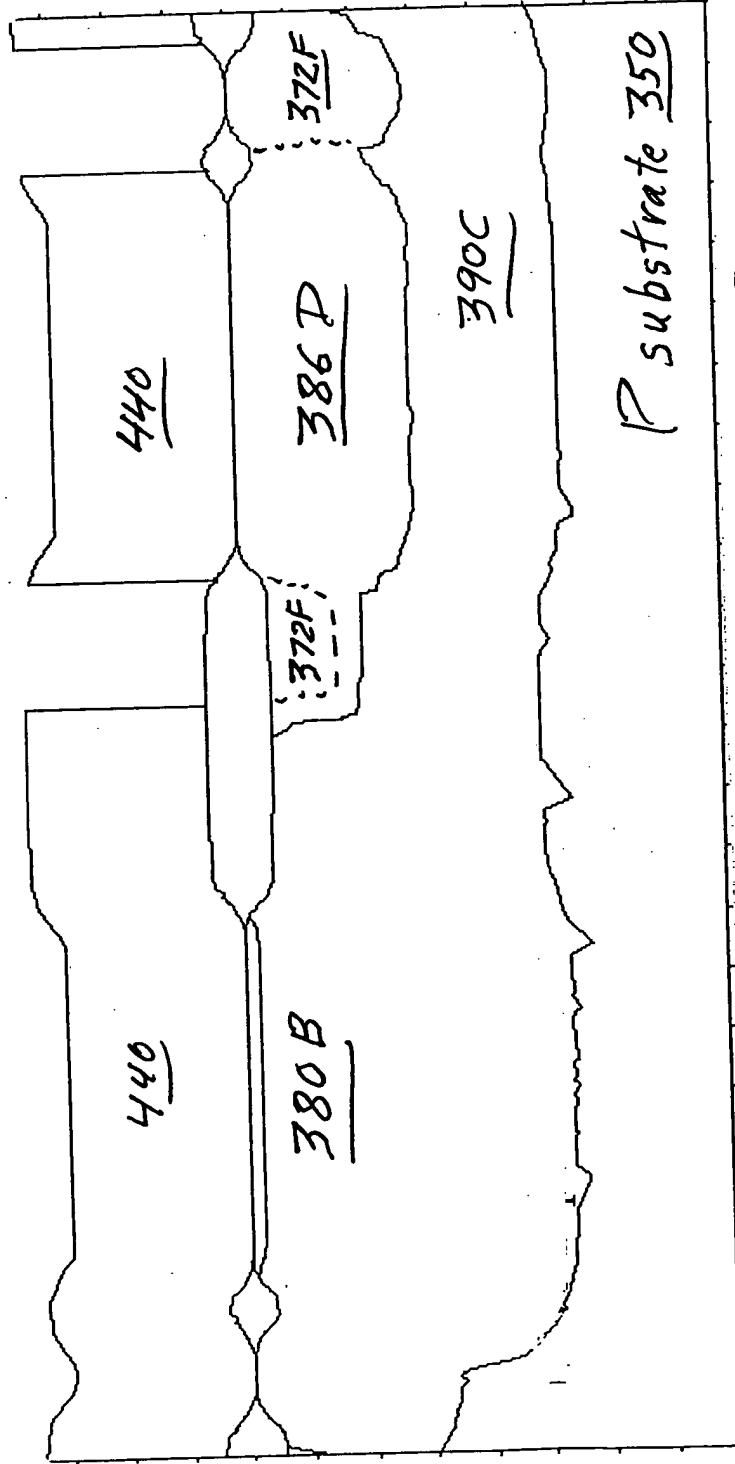
Conventional Layout  
 5V NPN 305      5V PNP 306



5V P Well Implant - Second Stage

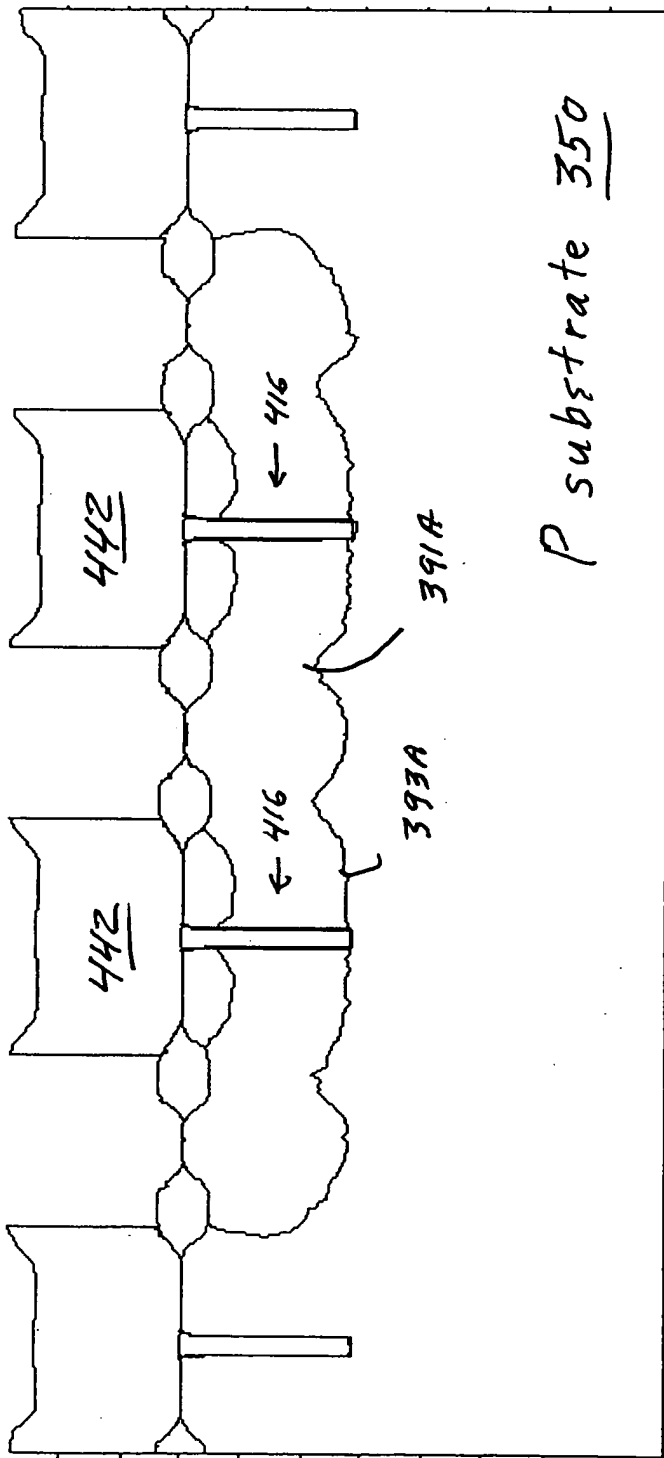
Fig. 46C

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



5V P Well Implant - Second Stage  
Fig. 46E

30V Lateral Trench Dmos 308

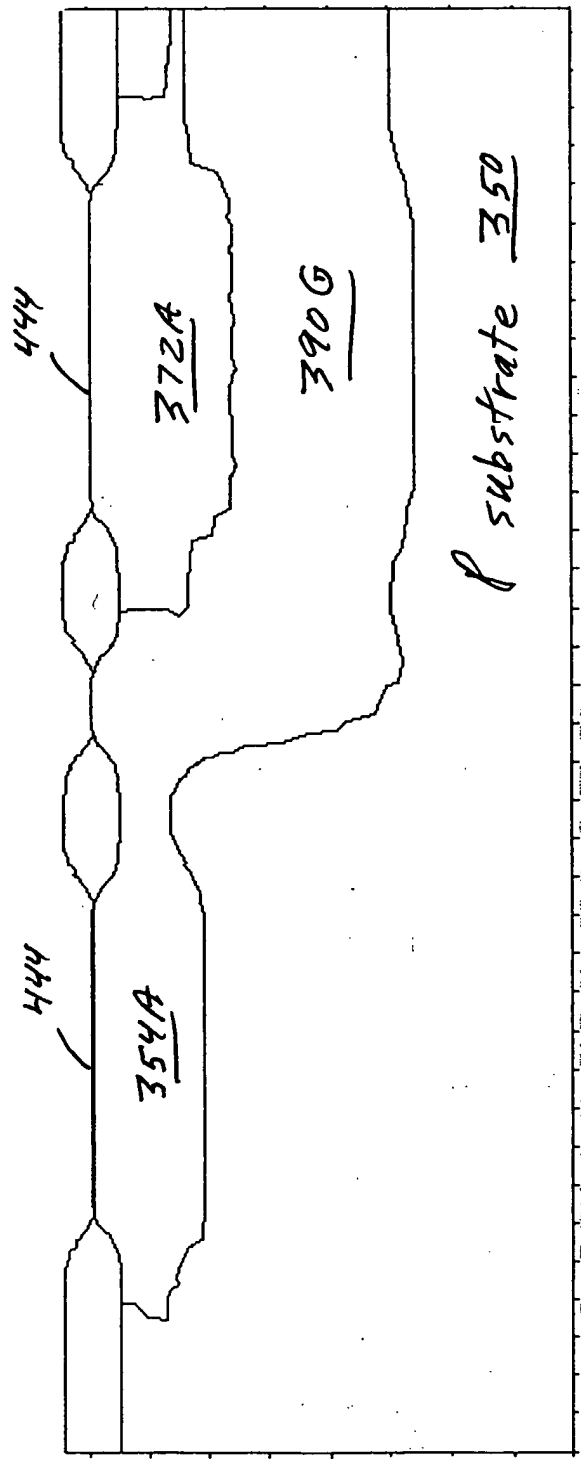


Etch-Block Mask and Etching of Planar Active Regions

Fig 47D

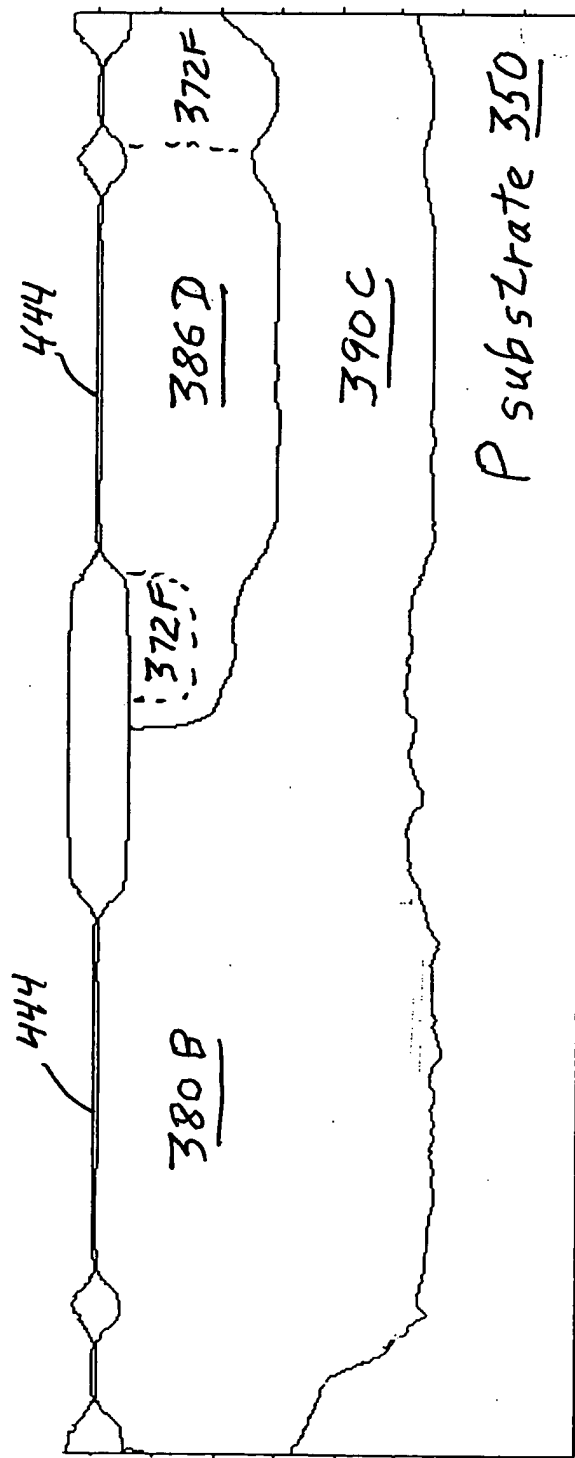
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5V PMOS 301      5V NMOS 302



First Planar Gate Oxide  
Fig. 42A

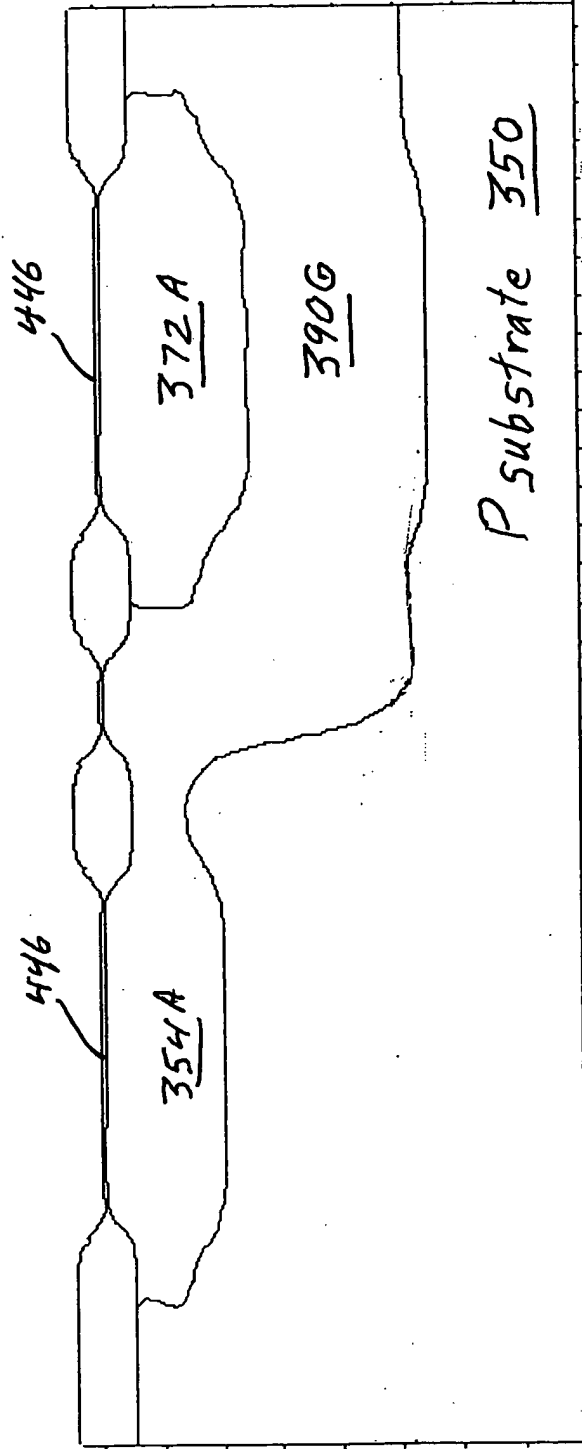
Symmetrical 12V CMOS  
12V PMOS 309 12V NMOS 310



First Planar Gate Oxide

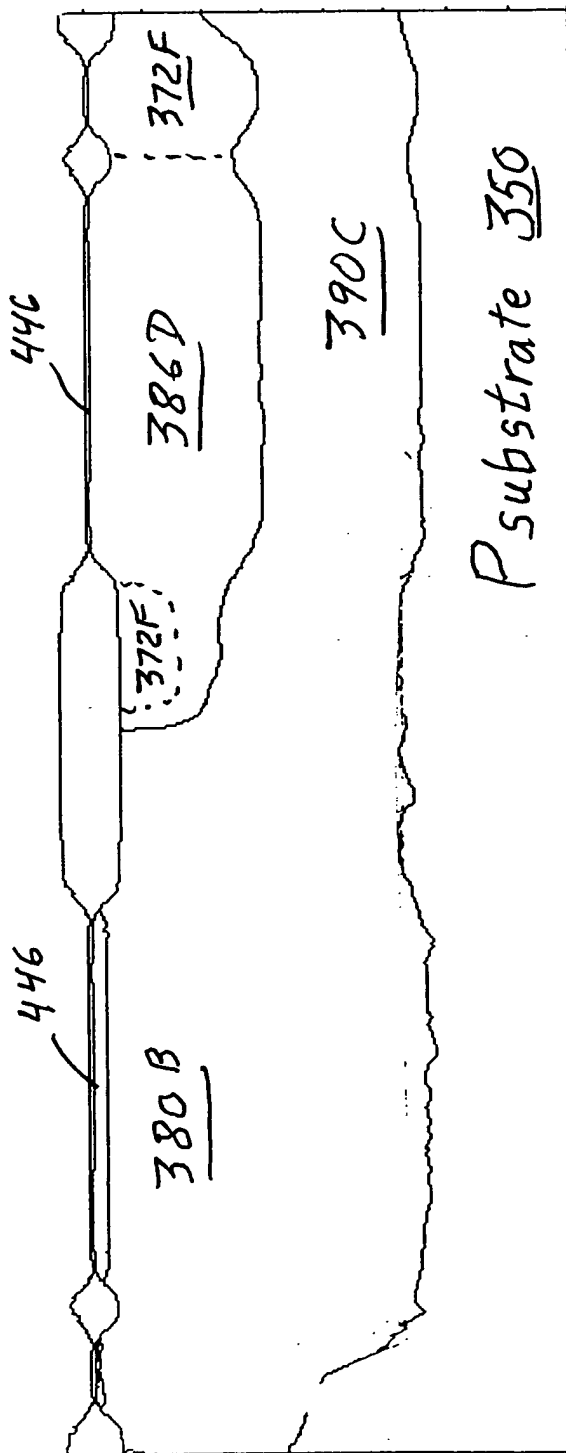


5V PMOS 301      5V NMOS 302



Threshold Adjust Implant - First Stage  
Fig. 49A

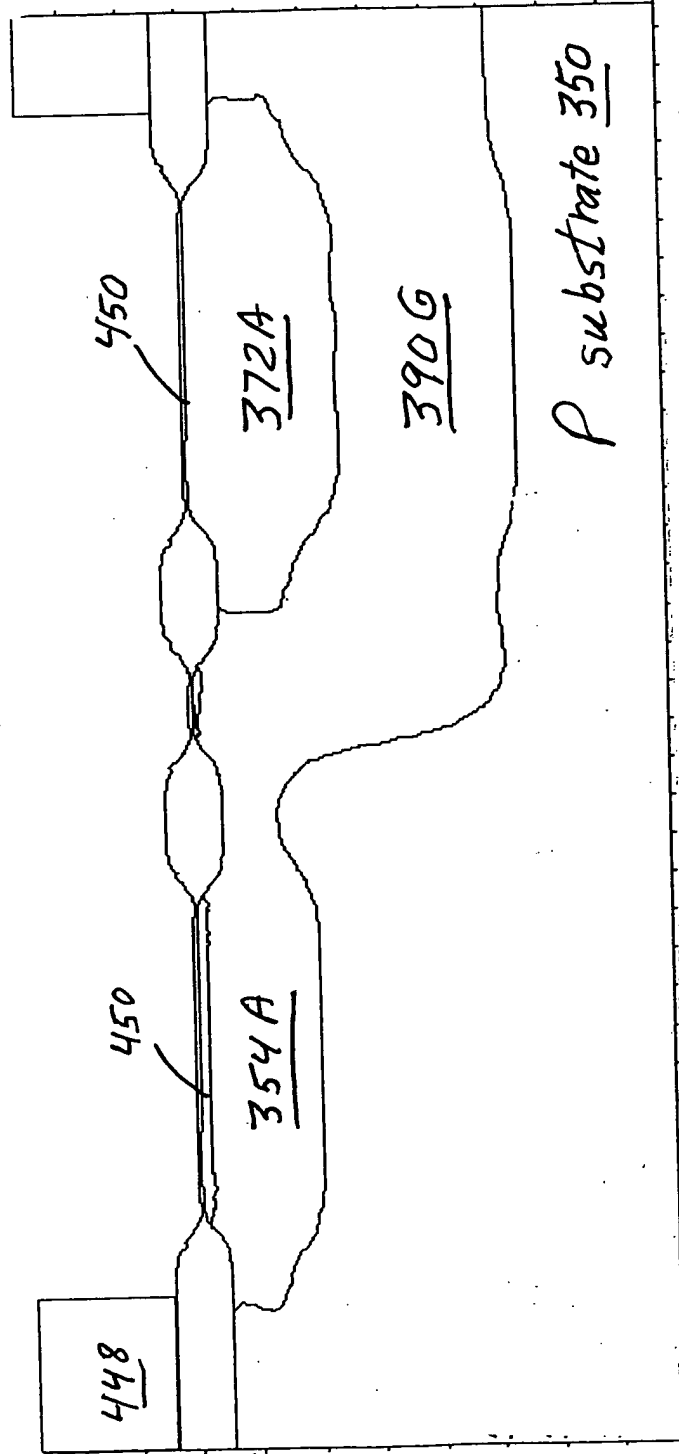
Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



Threshold Adjust Implant - First Stage  
Fig. 49E

5V NMOS 302

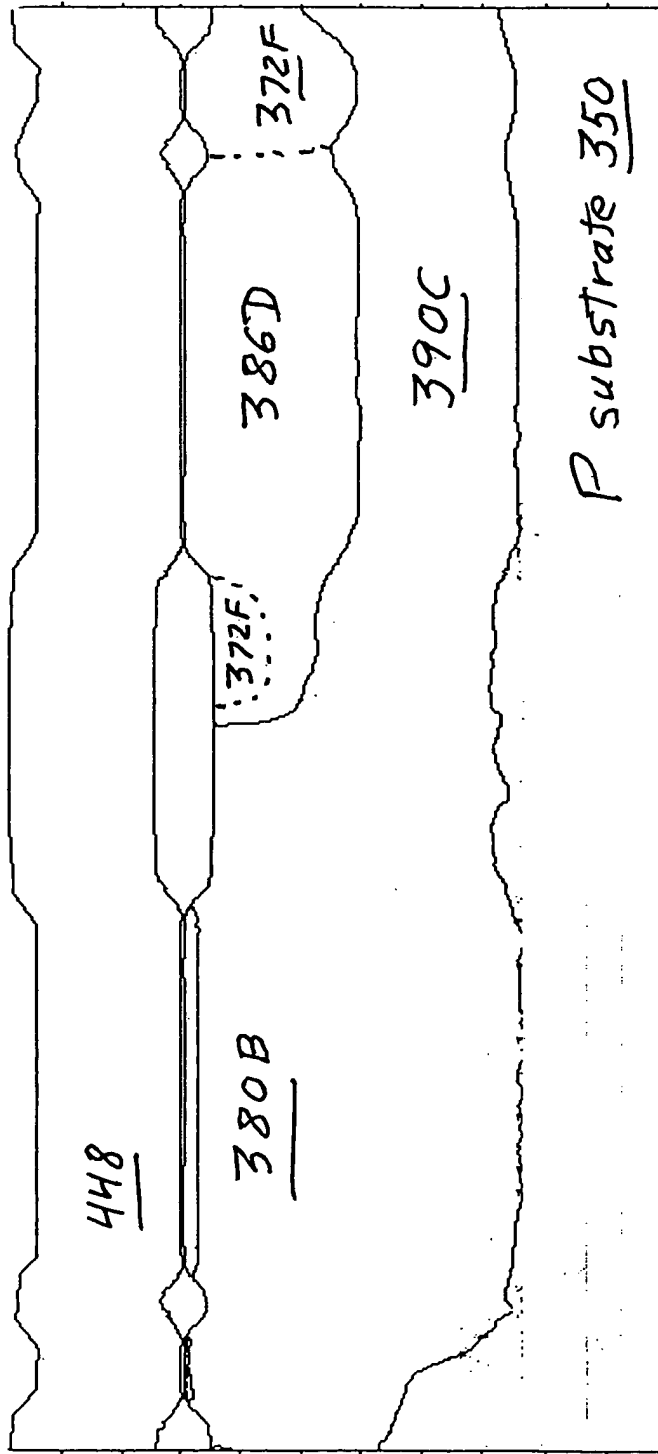
5V PMOS 301



Threshold Adjust Implant - Second Stage  
First Planar Gate Oxide Removal

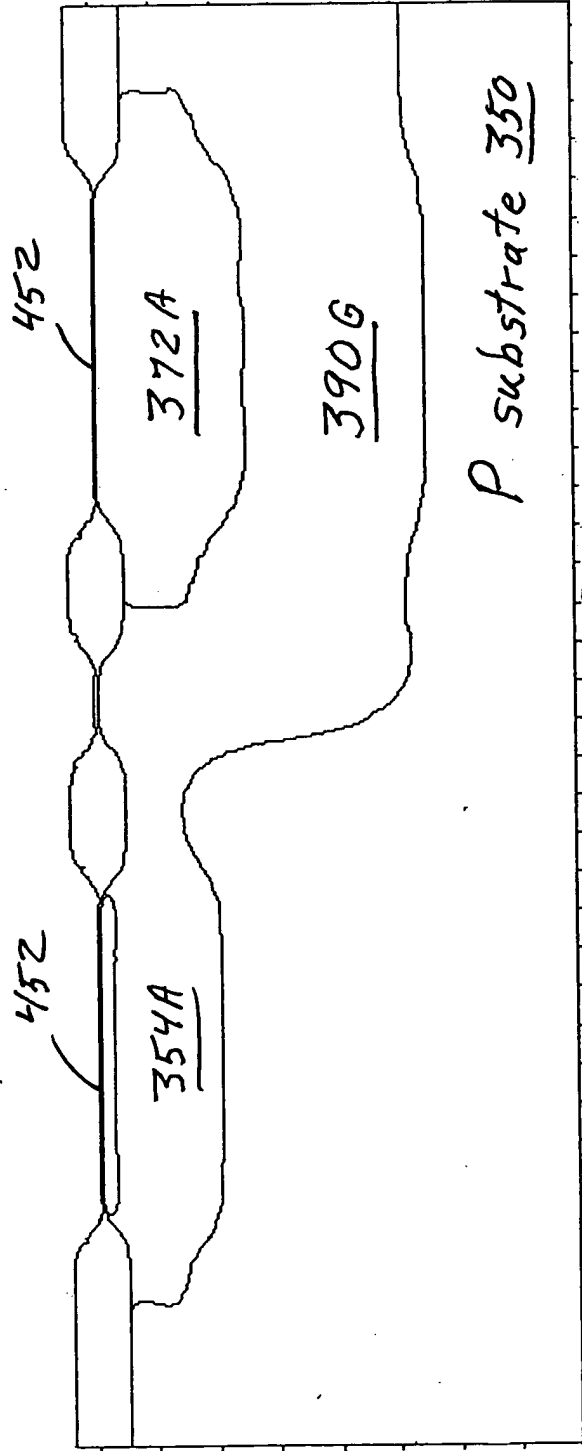
Fig. 50A

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



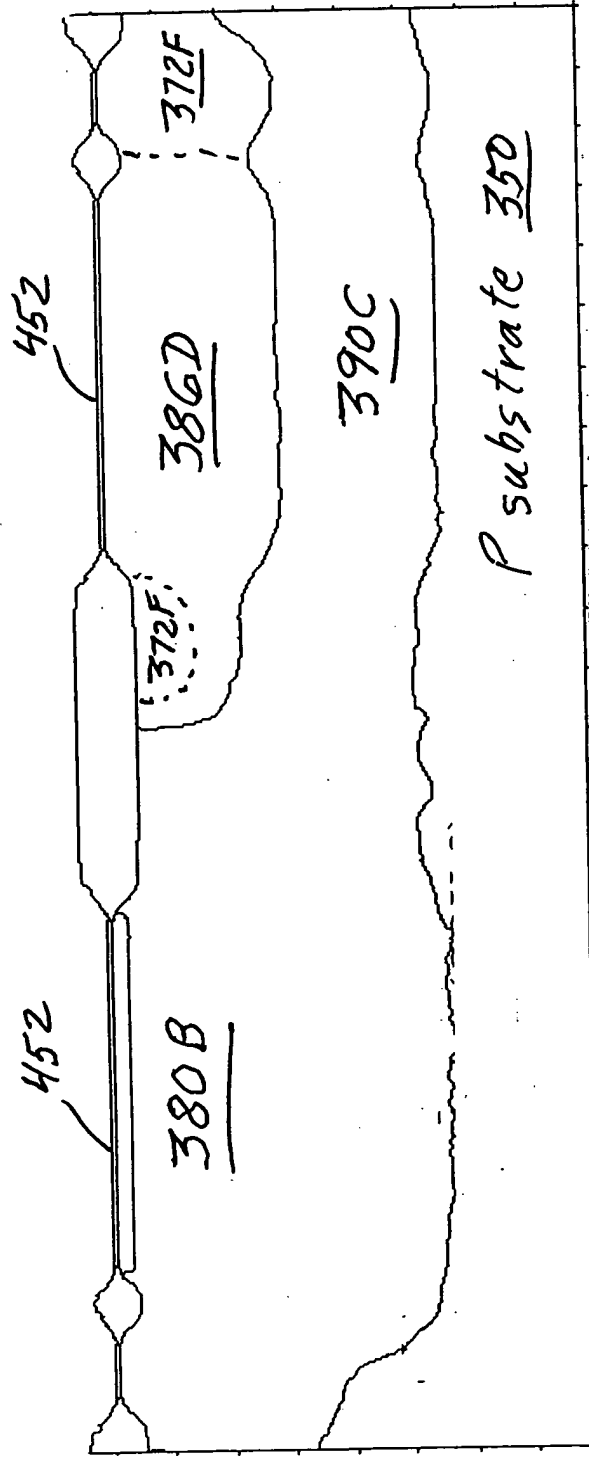
Threshold Adjust Implant - Second Stage  
Fig. 50E

5V PMOS 301      5V NMOS 302



Second Planar Gate Oxide  
Fig. 51A

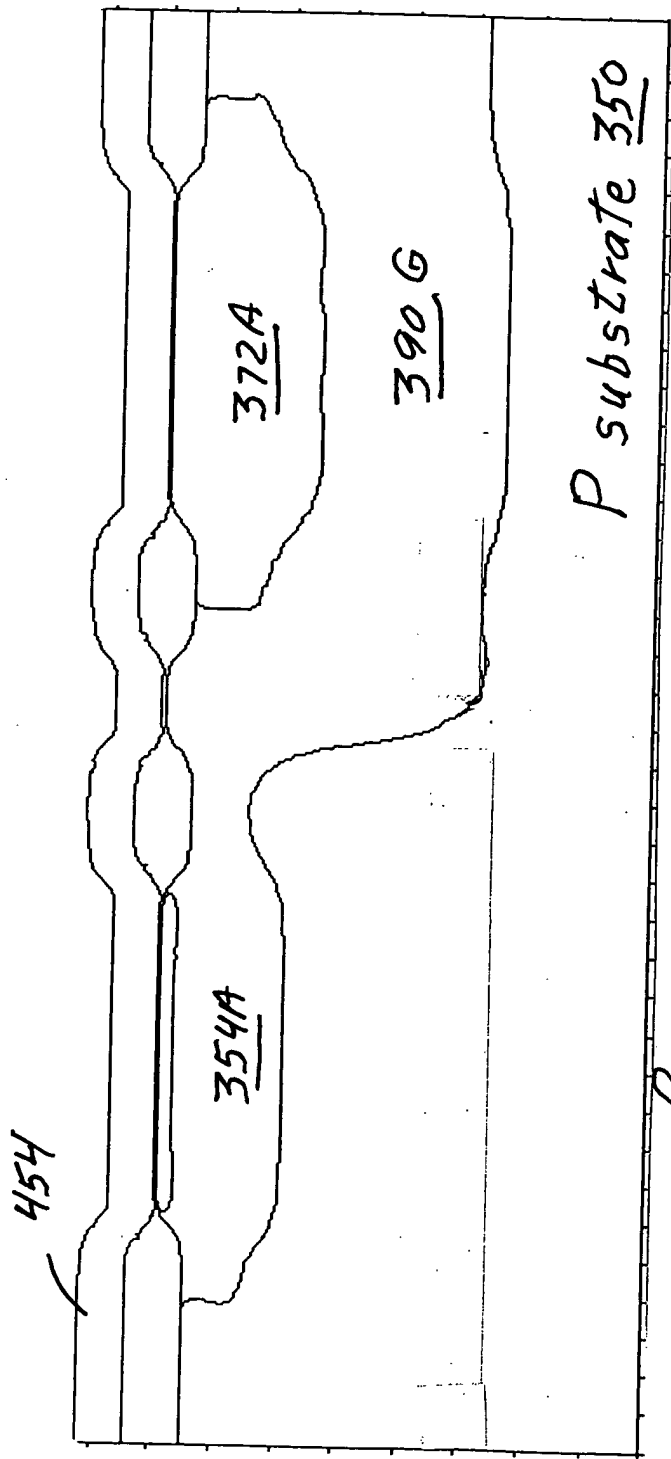
Symmetrical 12V CMOS 12V NMOS 310  
 12V PMOS 309



Second Planar Gate Oxide

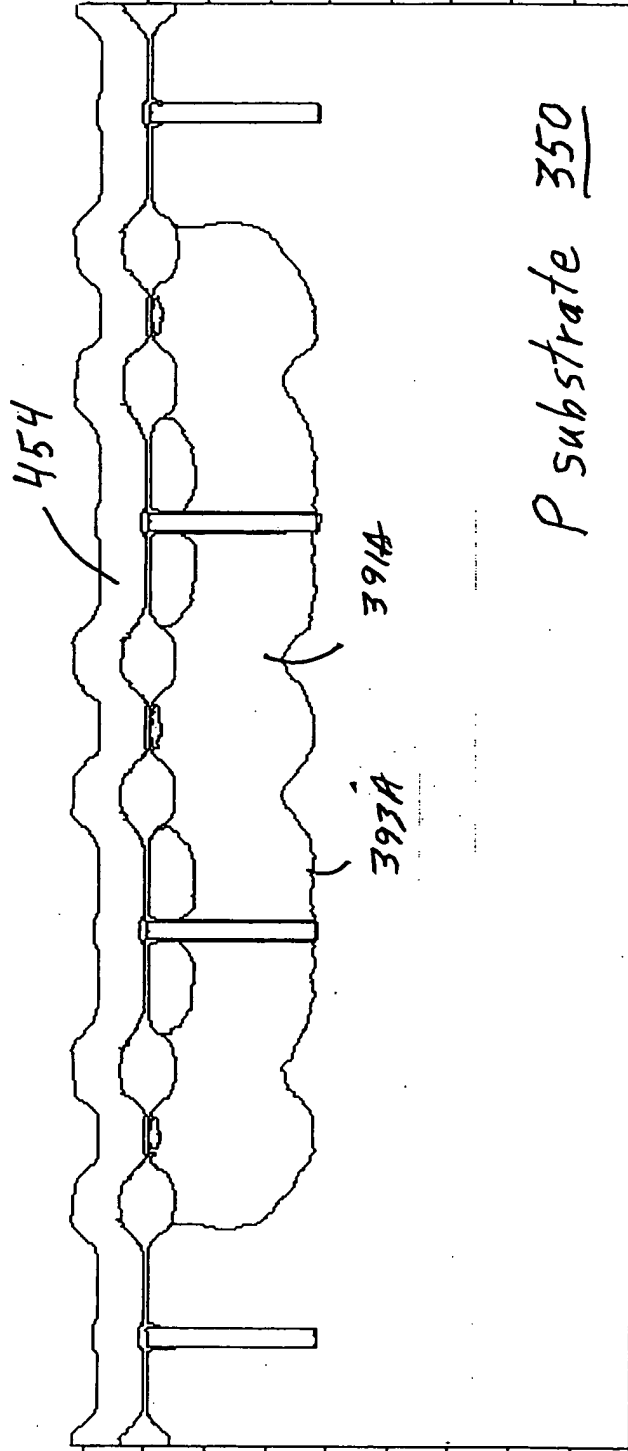
Fig. 51E

5V PMOS 301      5V NMOS 302



Polysilicon - Third Layer  
Fig. 52A

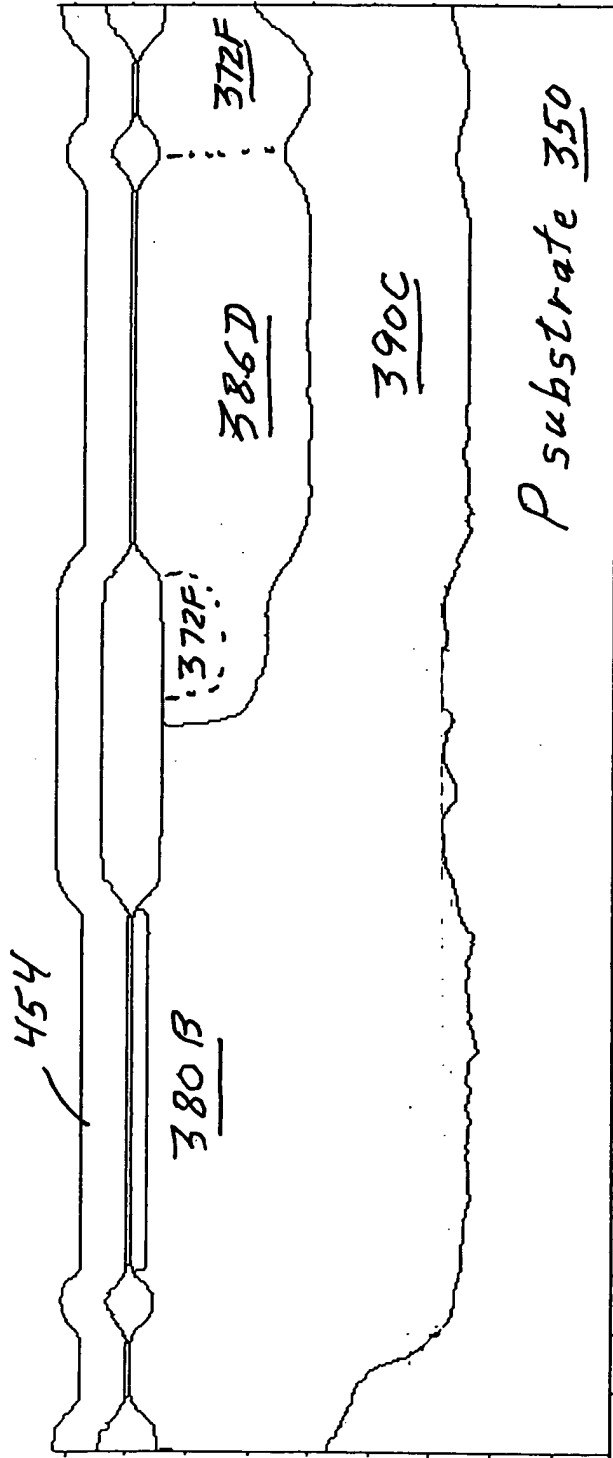
# 30V Lateral Trench DMOS 308



Polysilicon - Third Layer  
Fig. 52D

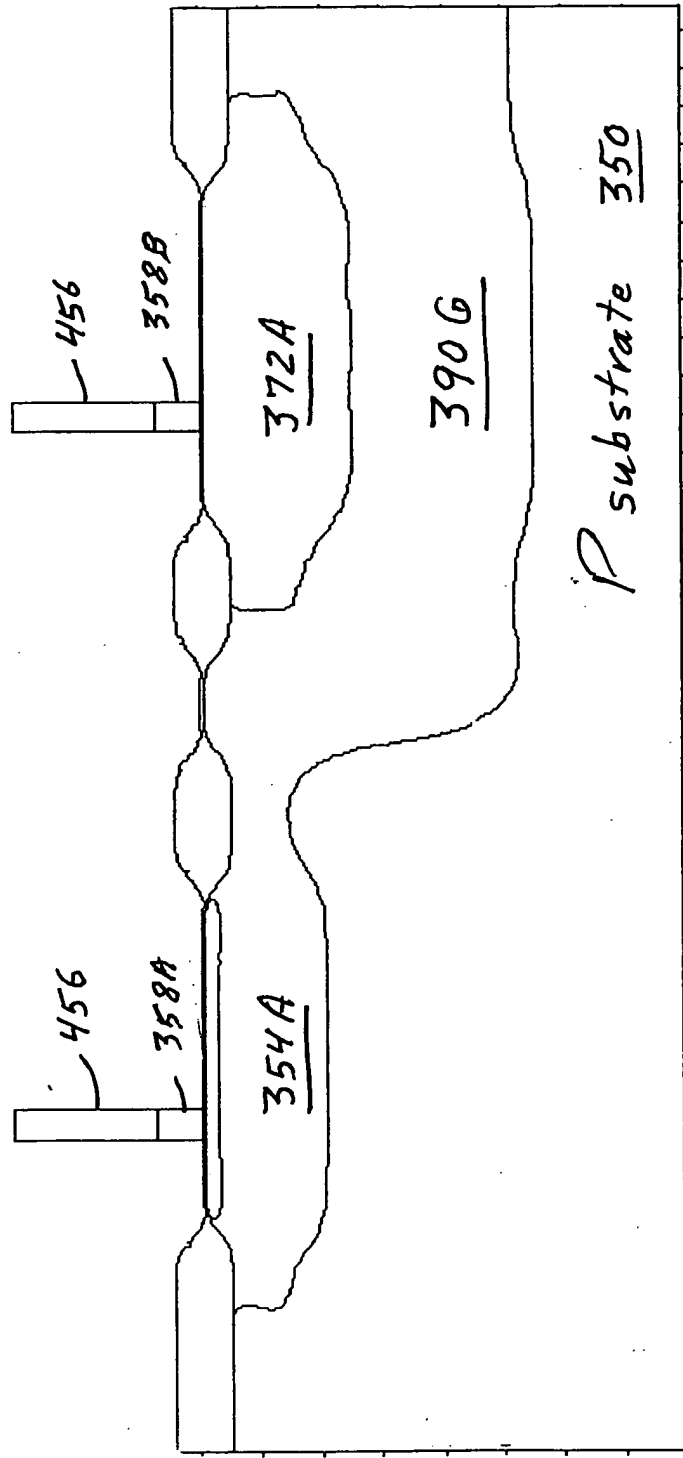


Symmetrical 12V CMOS  
 12V PMOS 309 12V NMOS 310



Polysilicon - Third Layer  
Fig. 52E

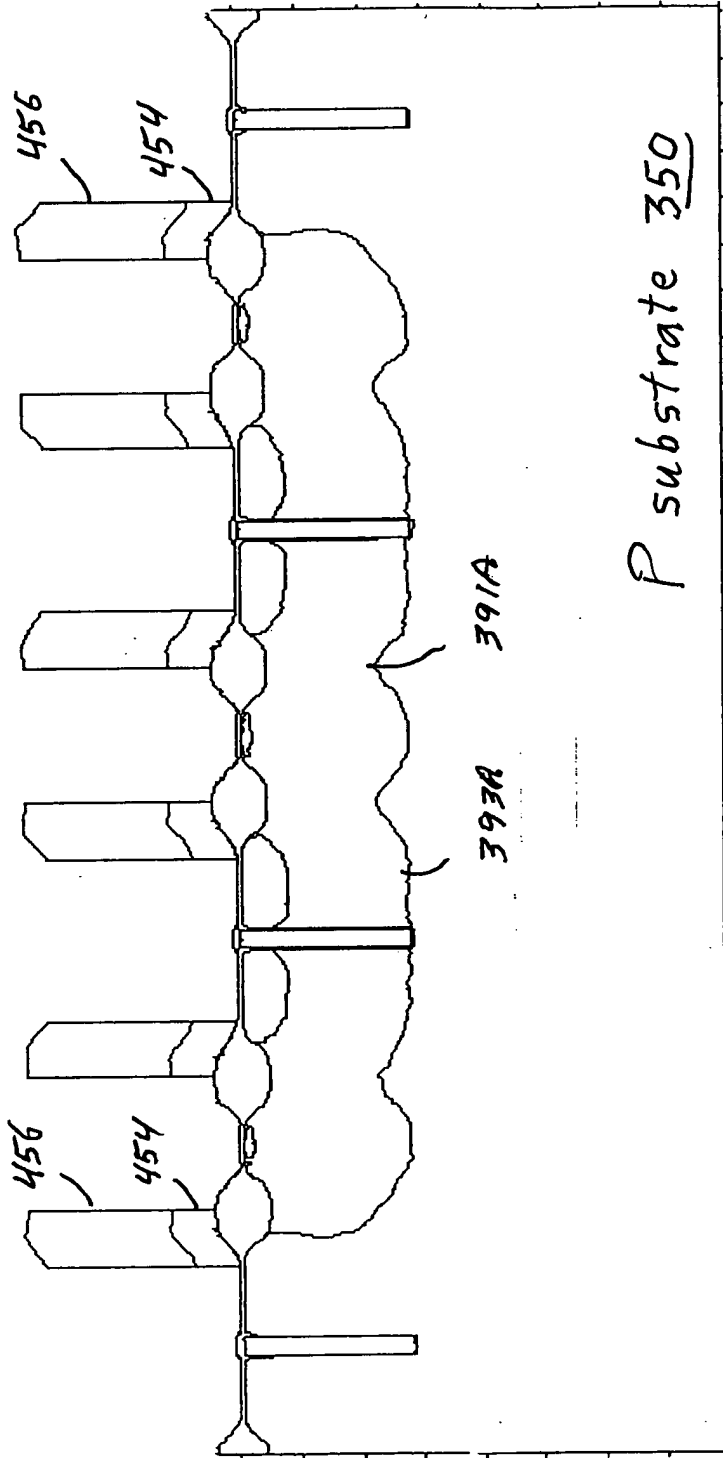
5V PMOS 301      5V NMOS 302



Planar Gate Formation  
Fig. 53A

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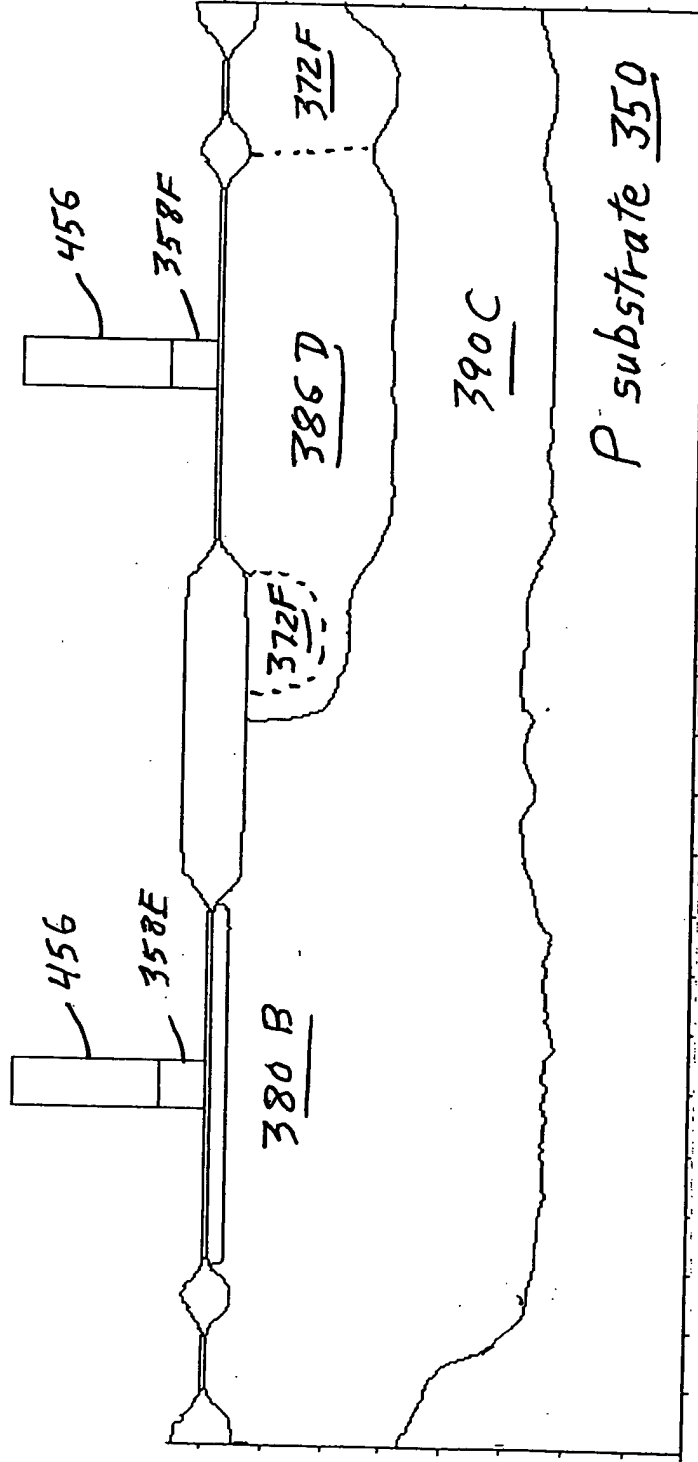
30V Lateral Trench DMOS 308



P substrate 350

Fig. 53D Planar Gate Formation

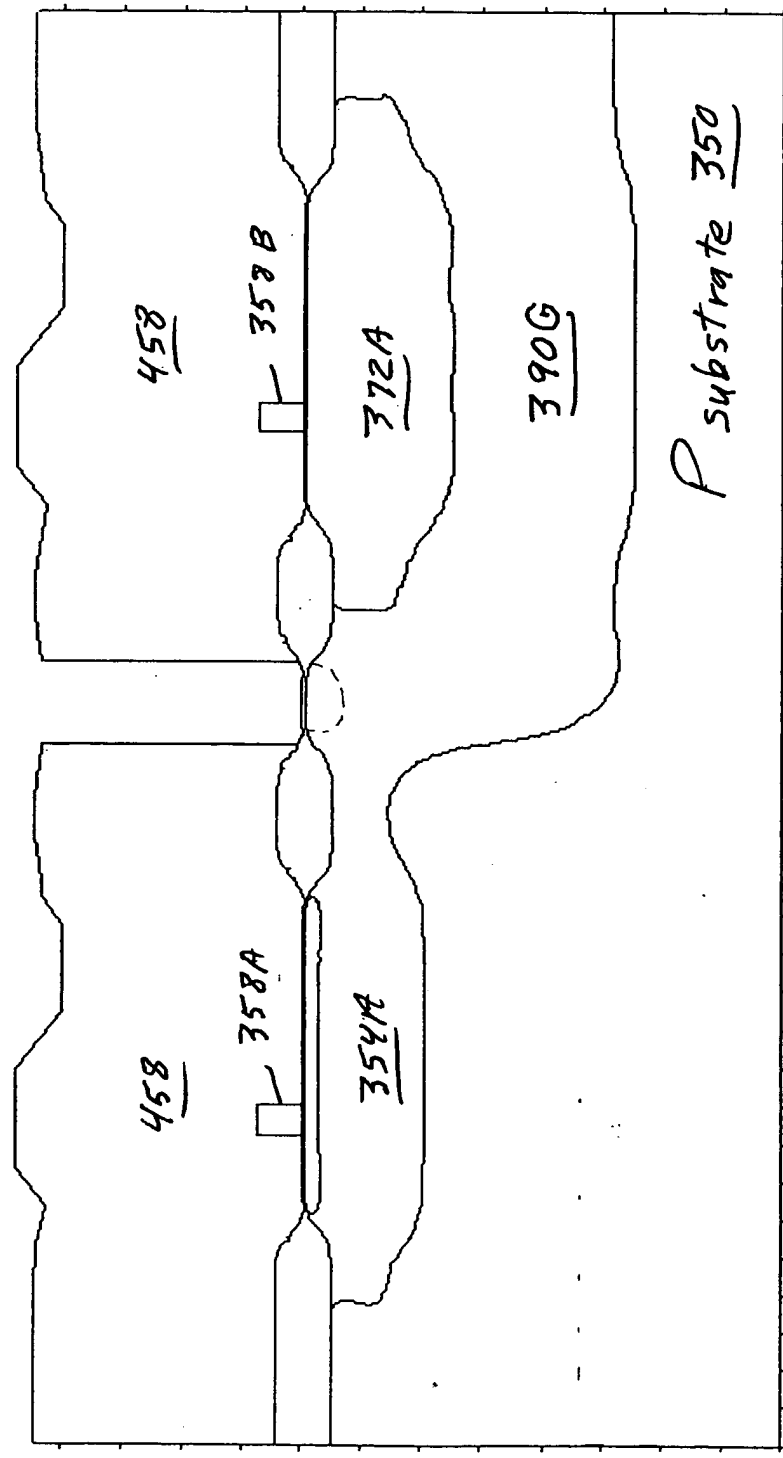
Symmetrical 12V CMOS  
 12V PMOS 309 12V NMOS 310



Planar Gate Formation

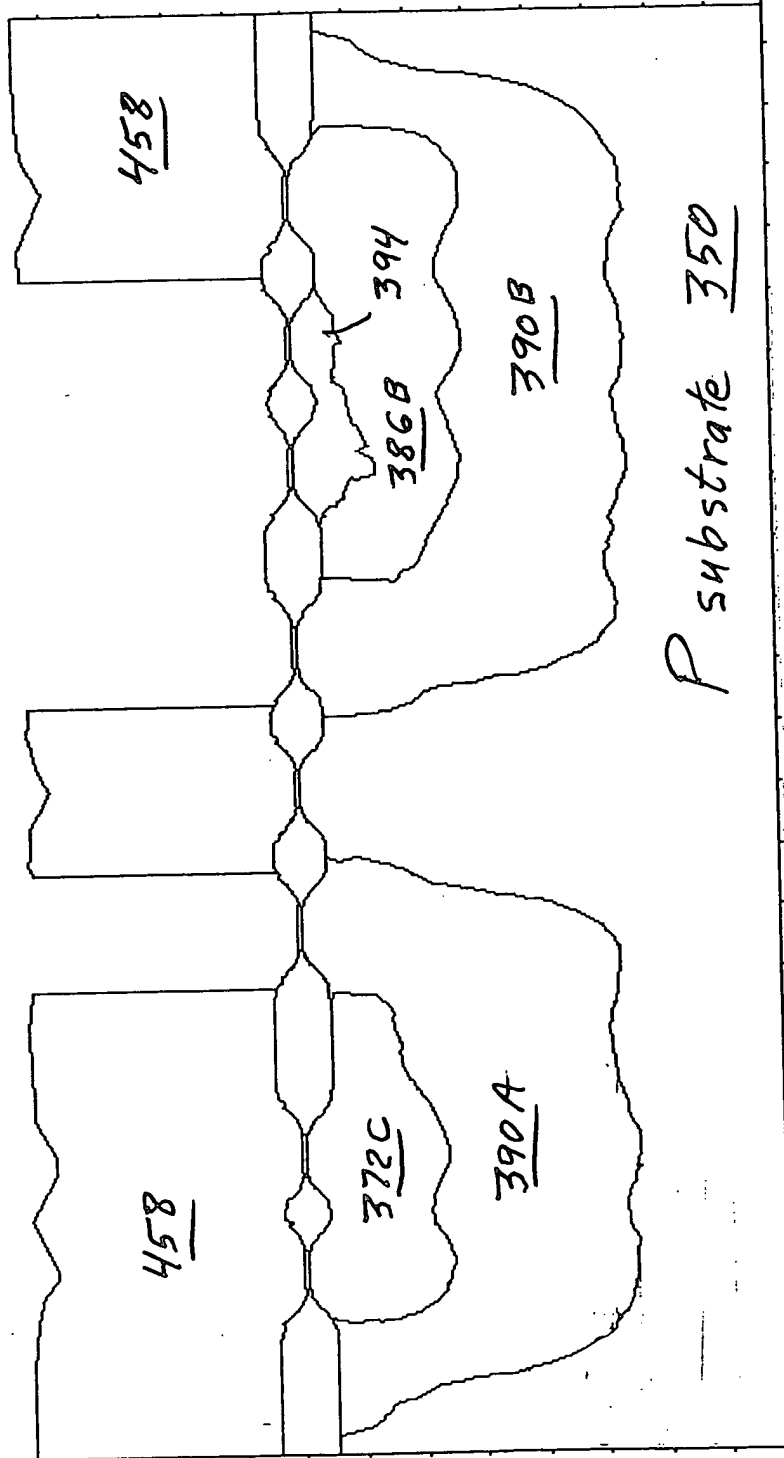
Fig 53E

5V PMOS 301      5V NMOS 302



N-Base Mask and Implant  
Fig. 54A

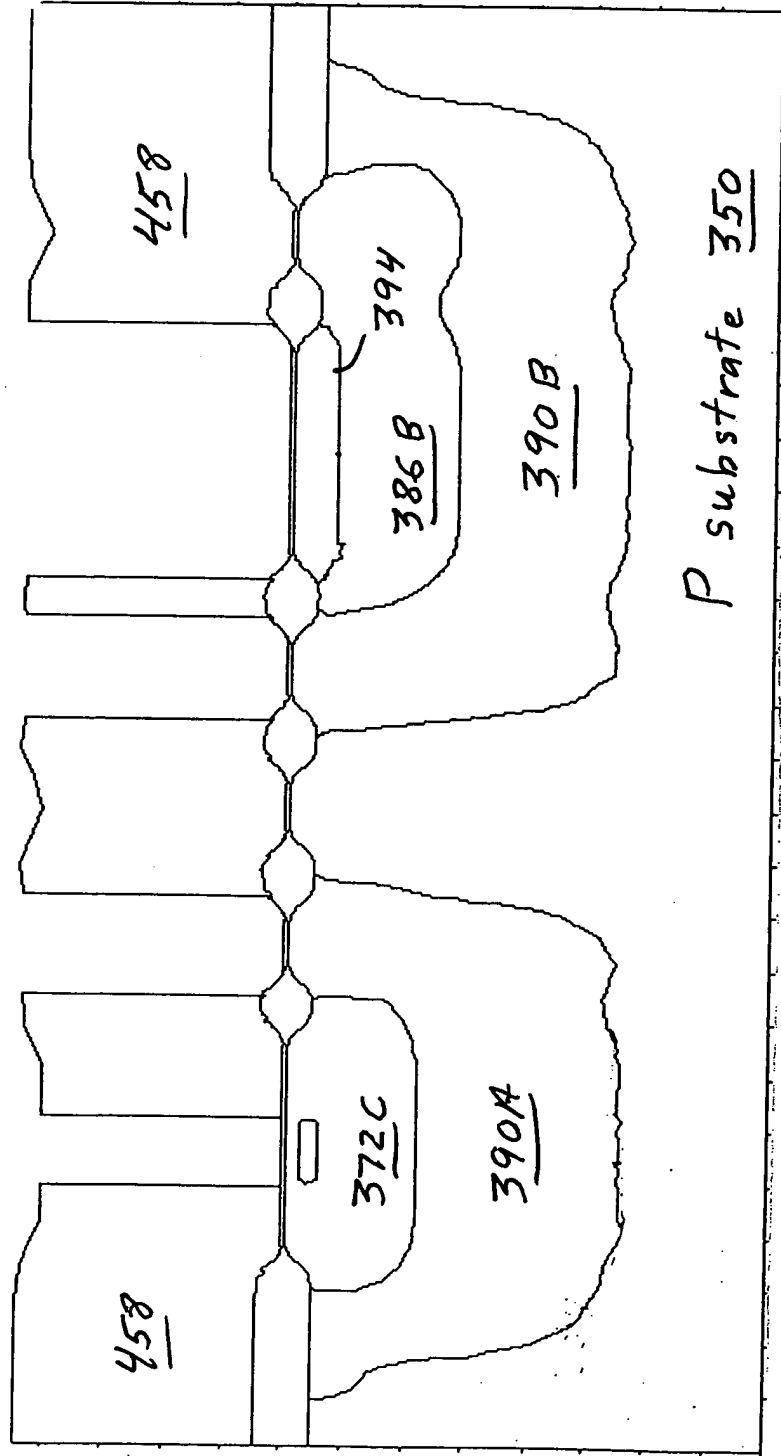
High F<sub>T</sub> Layout  
 5V NPN 305      5V PNP 306



N-Base Mask and Implant  
 Fig. 54B

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Conventional Layout  
5V NPN 305      5V PNP 306



N-Base Mask and Implant  
Fig. 54C

A hand-drawn schematic diagram of a semiconductor device structure. The diagram shows a cross-section of a substrate 350 with a series of vertical pillars 393A and 393B. The pillars are connected by a horizontal layer 454. The pillars are labeled 456, 455, 454, 453, and 452 from left to right. The substrate is labeled 350. The pillars are labeled 393A and 393B. The horizontal layer is labeled 454. The pillars are labeled 456, 455, 454, 453, and 452 from left to right.

$P_{\text{substrate } 350}$

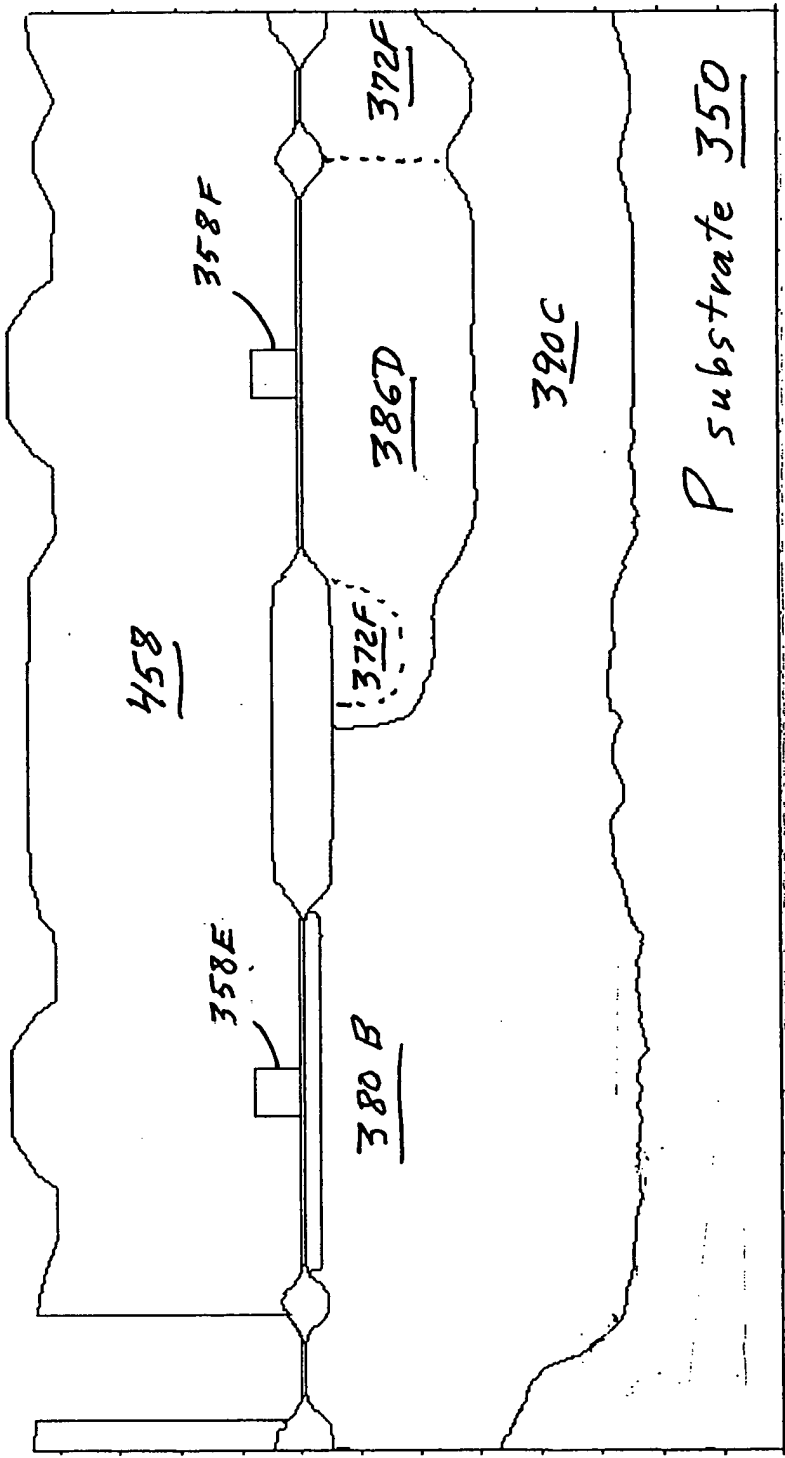
# N-Base Mask and Implant

Fig. 54D

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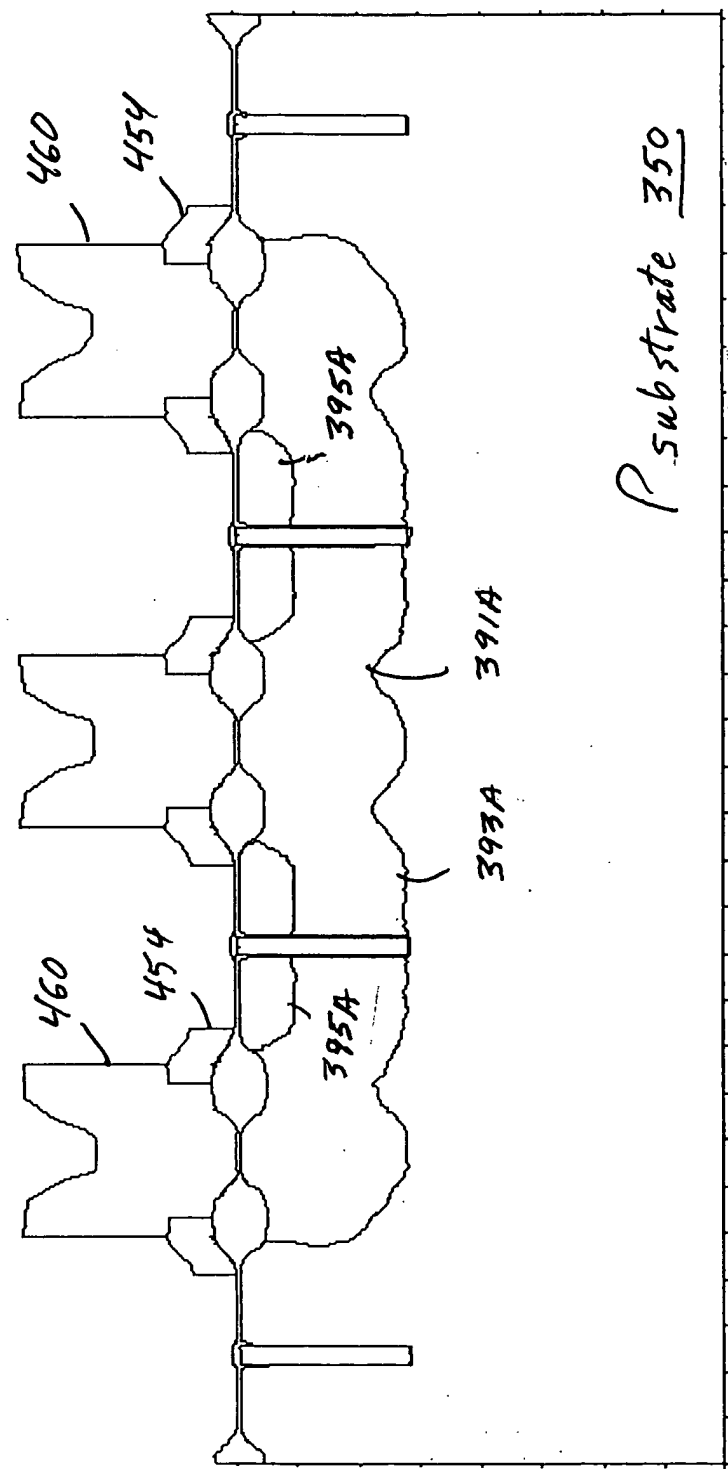


Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



N-Base Mask and Implant  
Fig. 54E

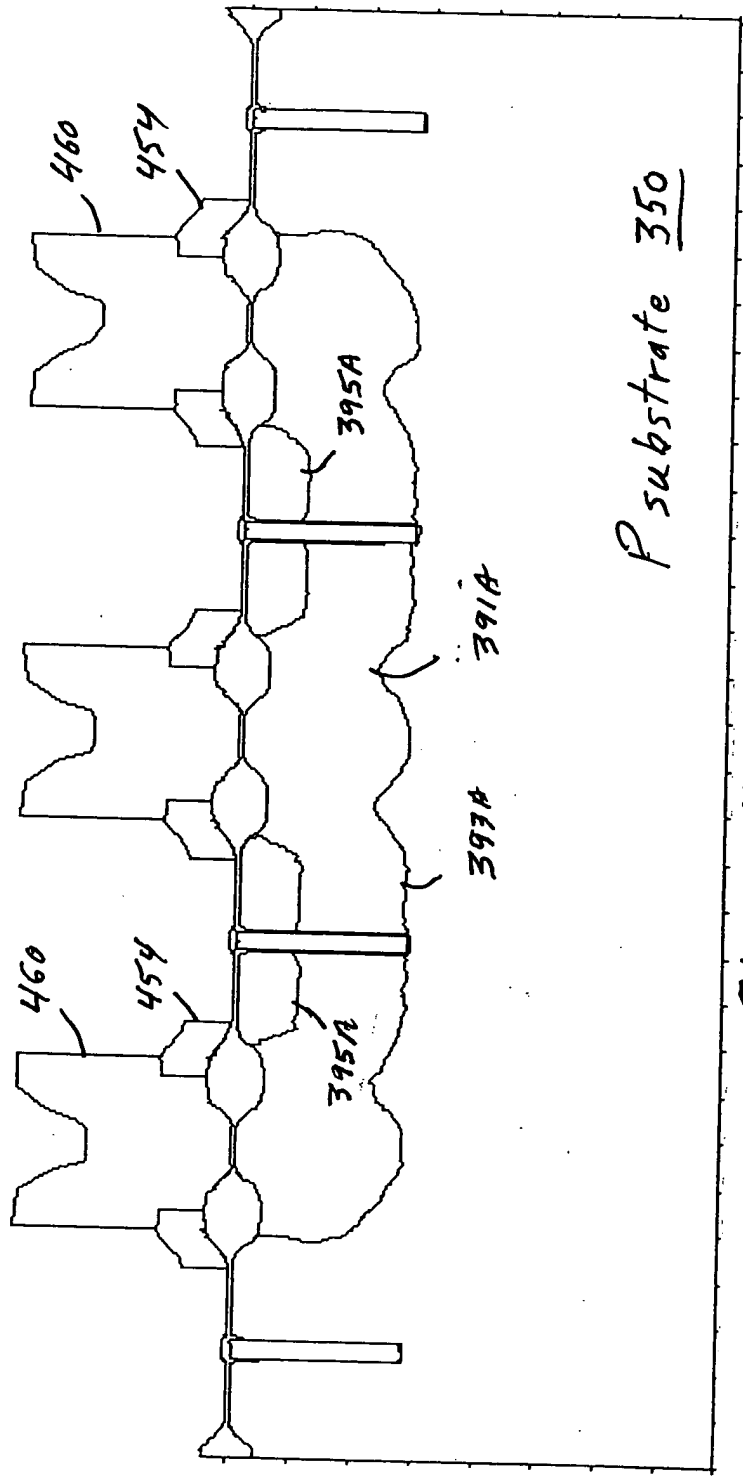
30V Lateral Trench DMOS 308



P Body Mask and Implant - First Stage  
Fig. 55D

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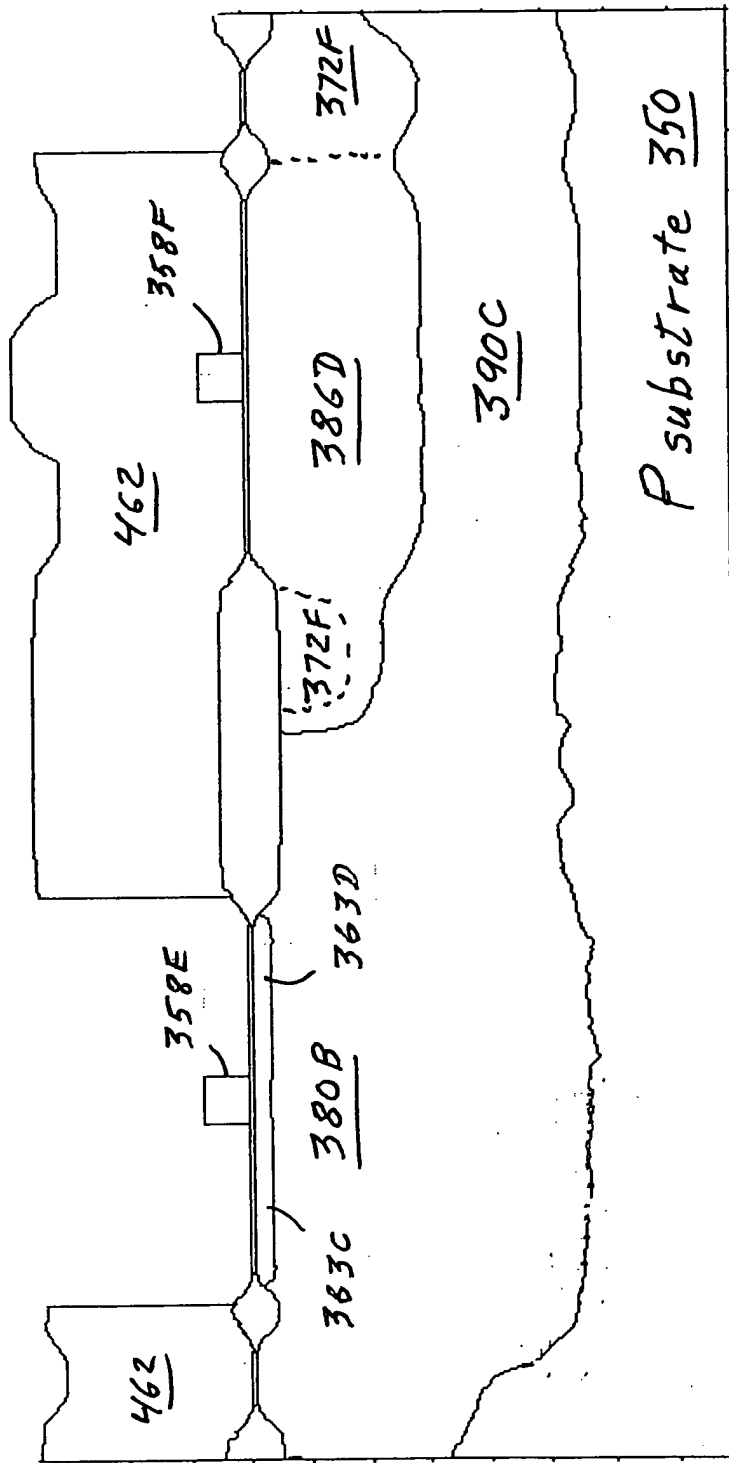
# 30V Lateral Trench DMOS 308



P substrate 350

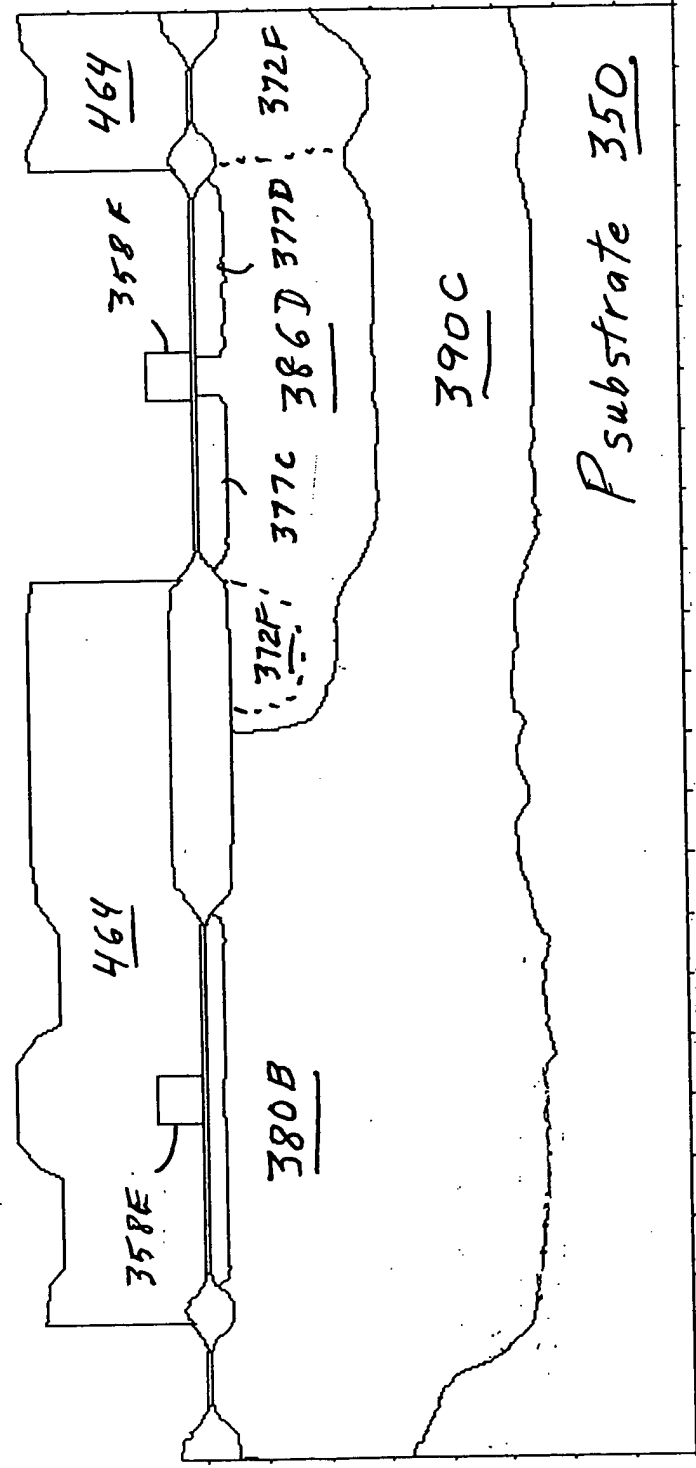
P body Mask and Implant - Second Stage  
Fig. 56 D

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



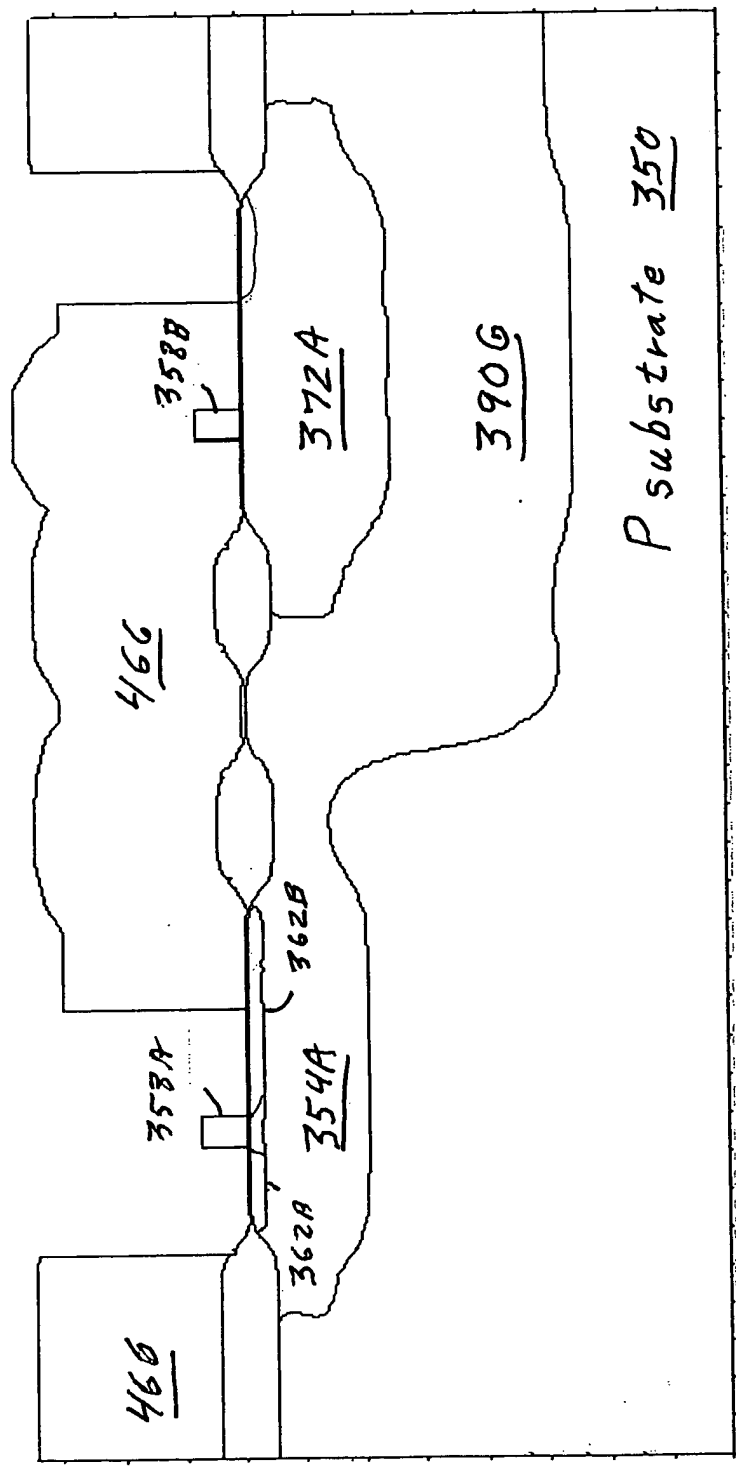
12V PLDD Implant  
 Fig. 57E

Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



12V N-LDD Implant  
Fig. 58E

5V PMOS 301      5V NMOS 302

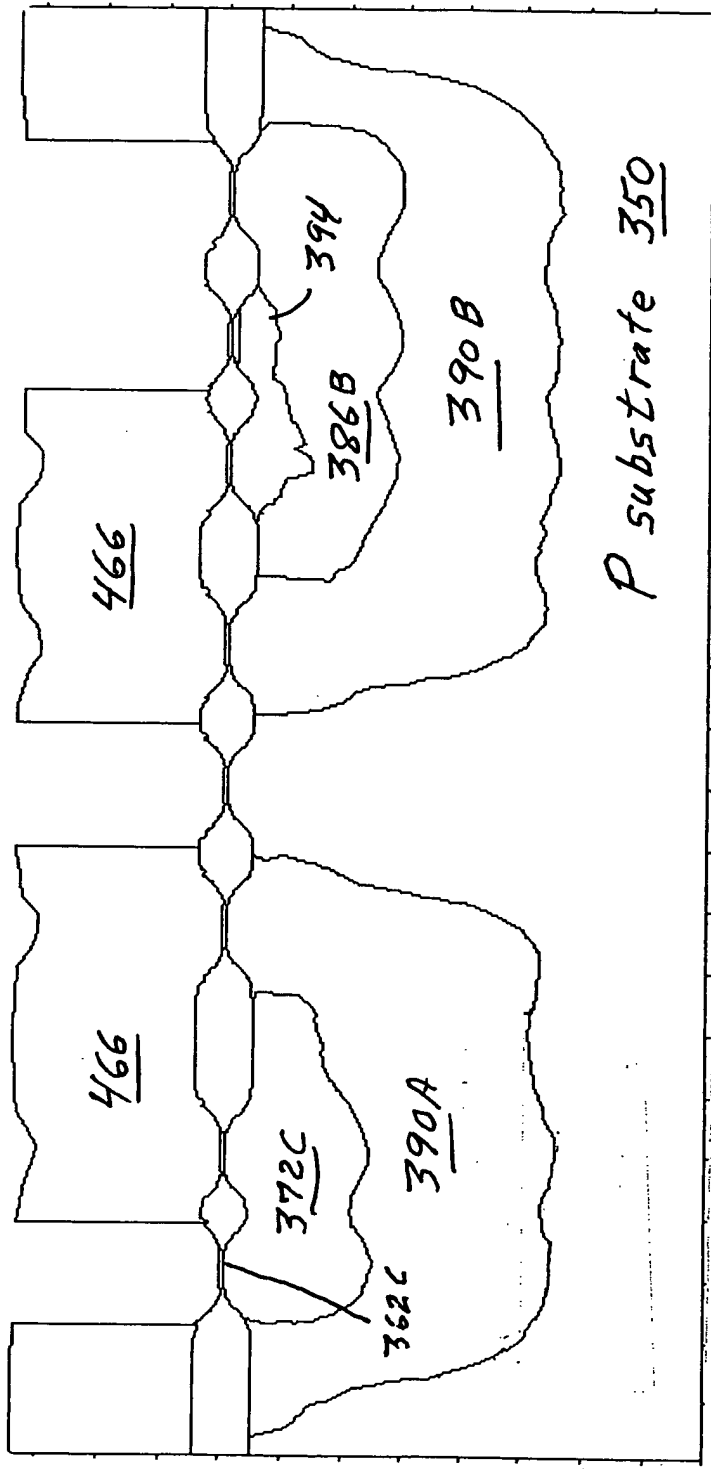


5V P-LDD Implant

Fig. 59A

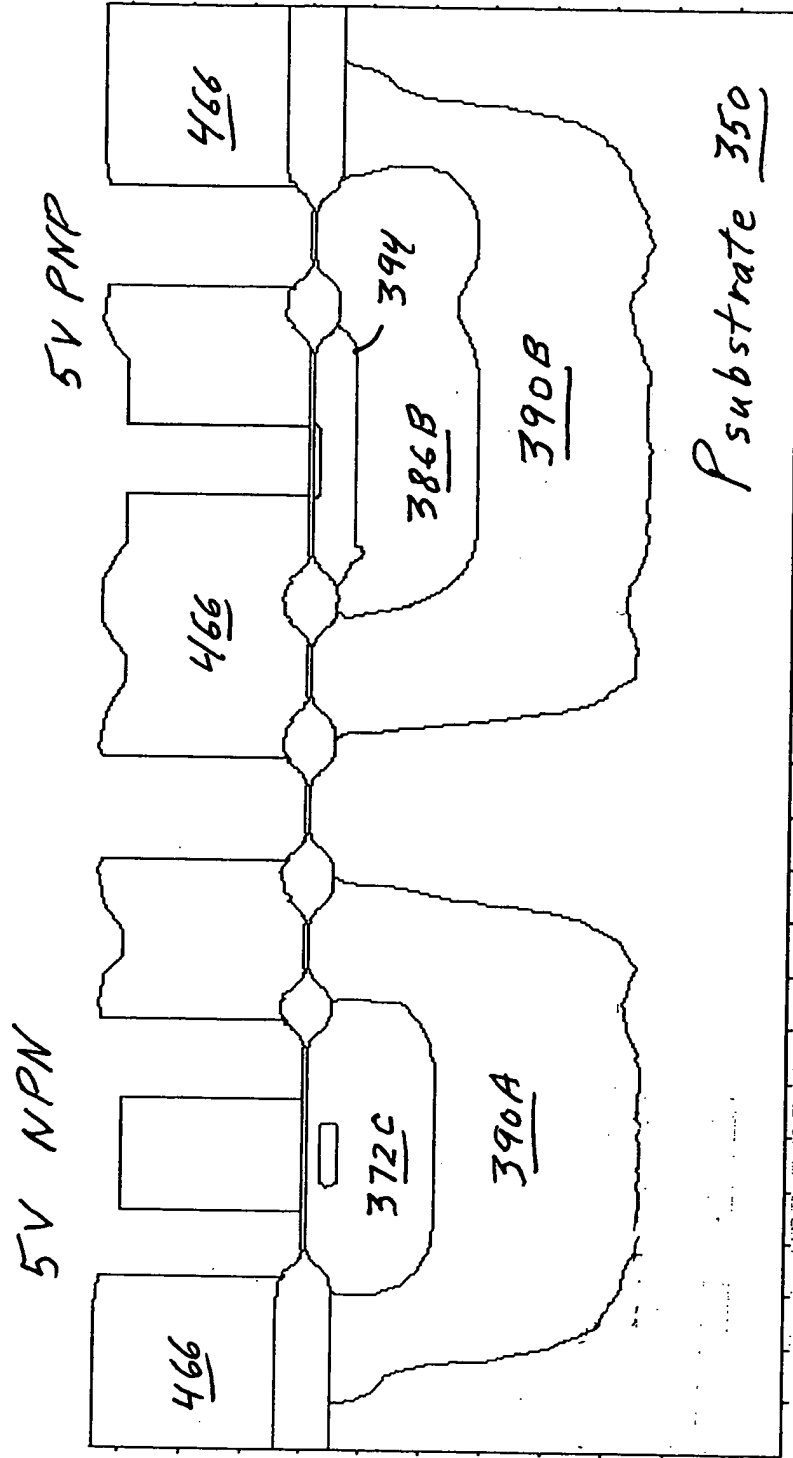
# High F<sub>T</sub> Layout

5V NPN 305      5V PNP 306



5V P-LDD Implant  
Fig. 59B

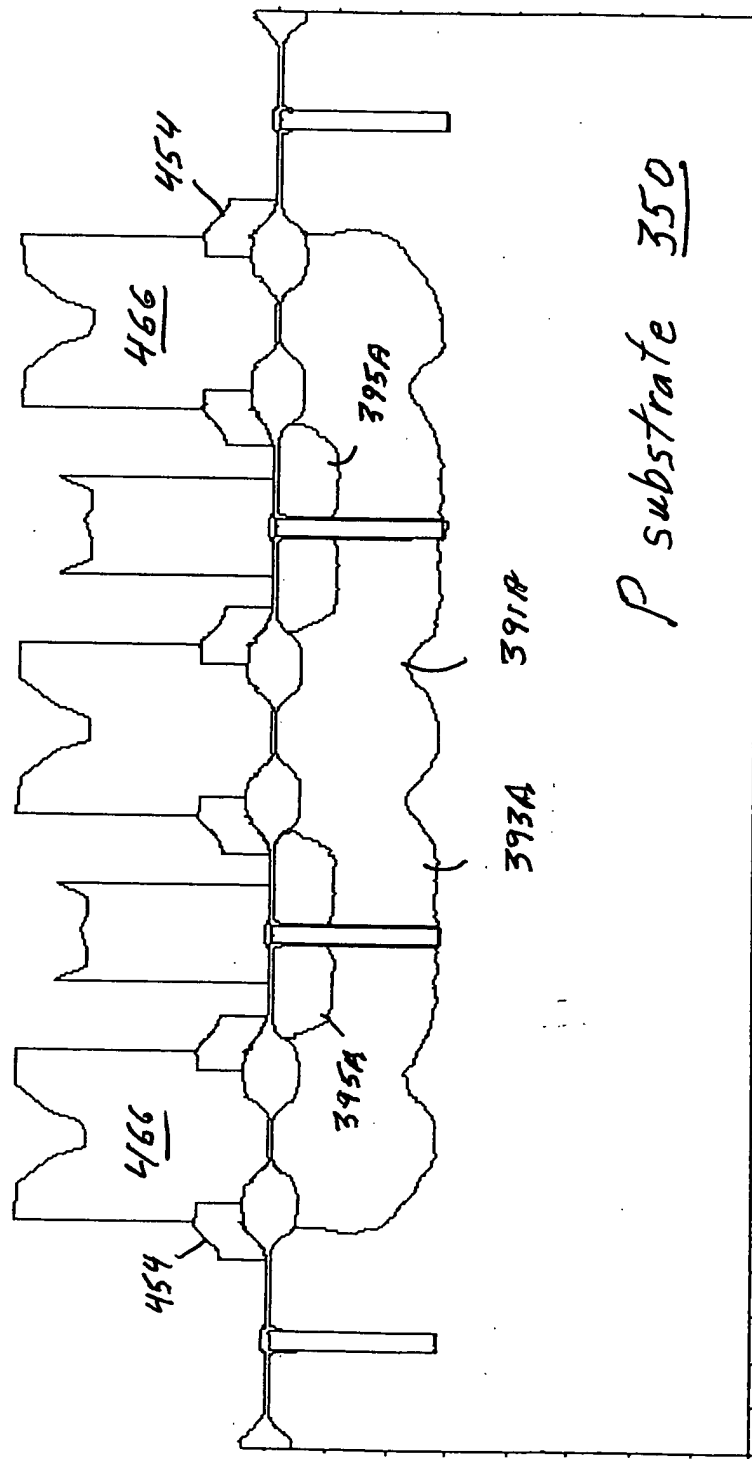
# Conventional Layout



5V P-LDD Implant  
Fig. 59C



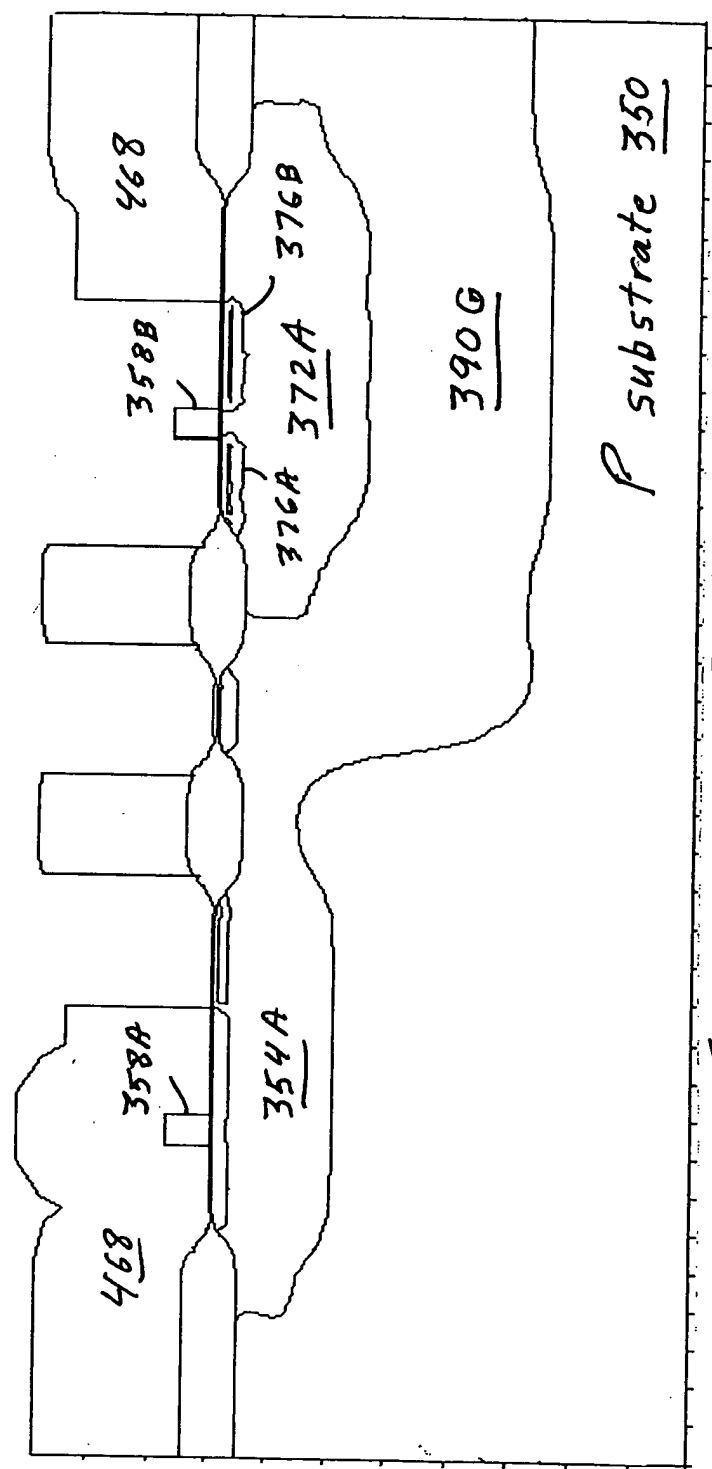
# 30V Lateral Trench DMOS 308



P substrate 350

5V P-LDD Implant  
Fig. 59D

5V PMOS 301      5V NMOS 302

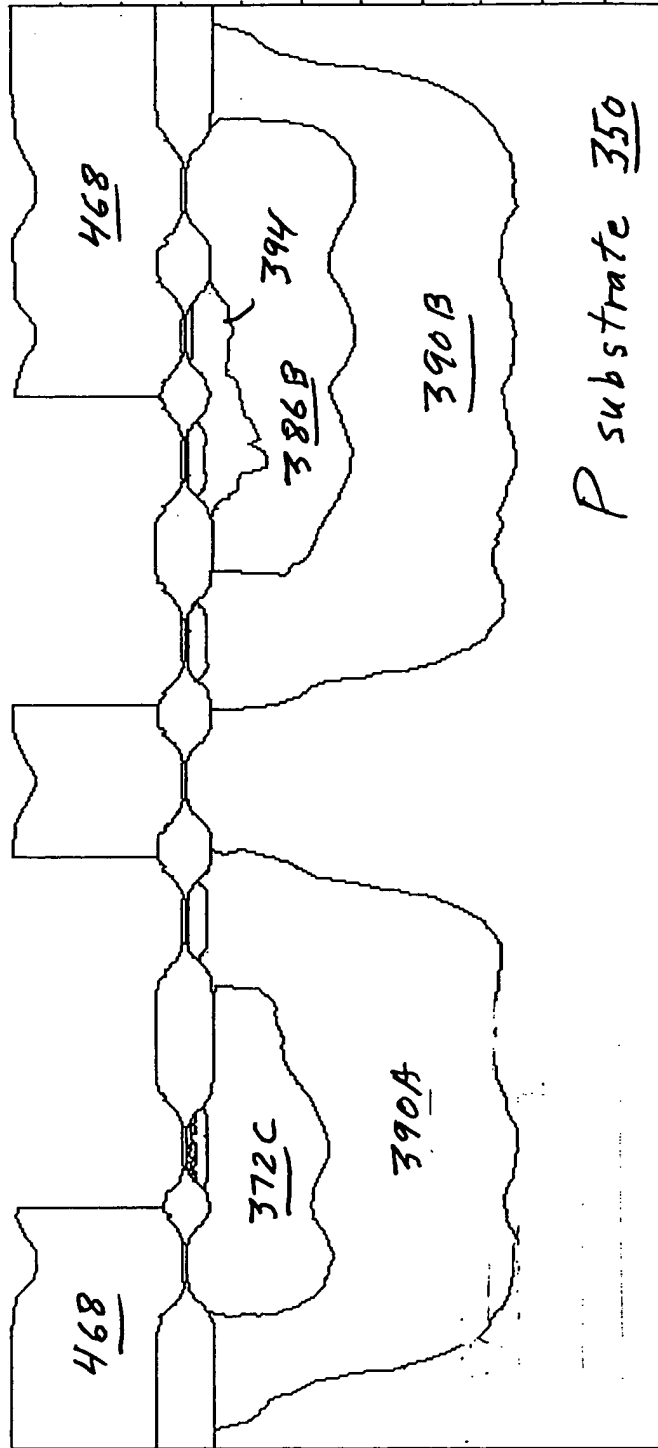


5V N-LDD Implant  
Fig. 60A

# High F<sub>T</sub> Layout

5V NPN 305

5V PNP 306



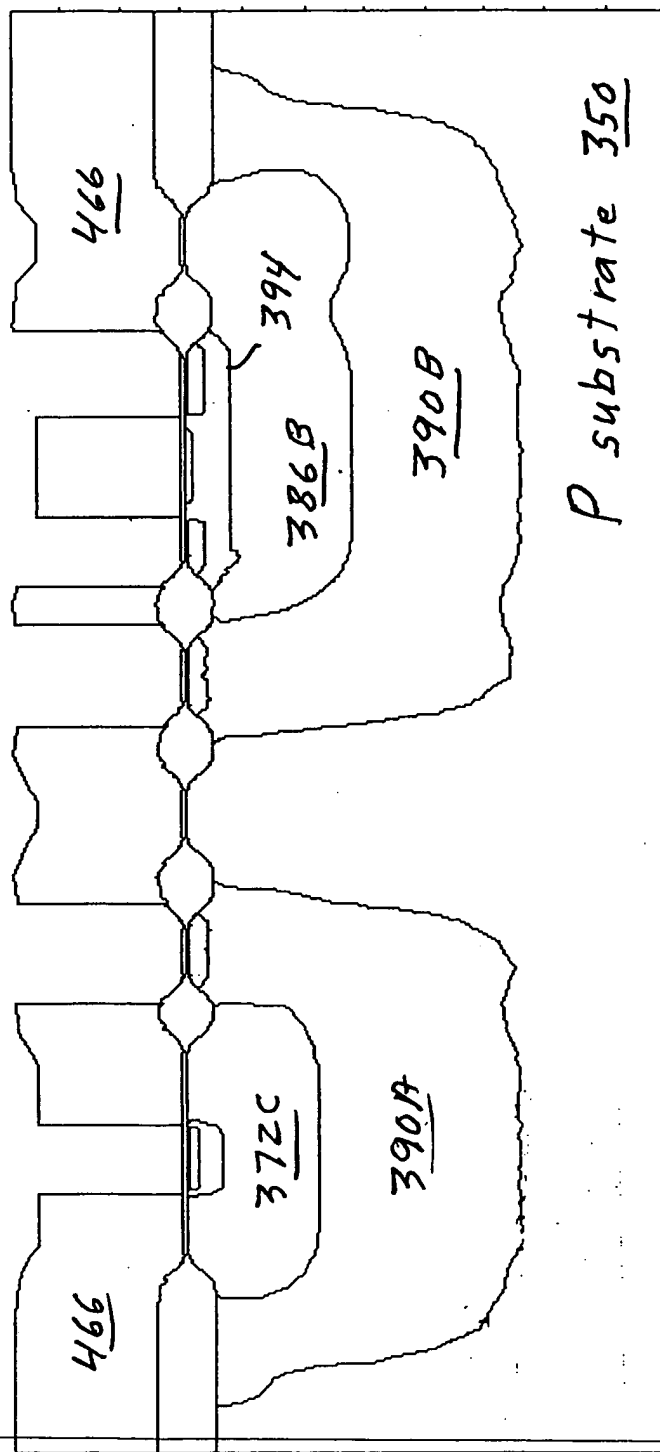
5V N-LDD Implant

Fig 60B

Conventional Layout

5V NPN

5V PNP

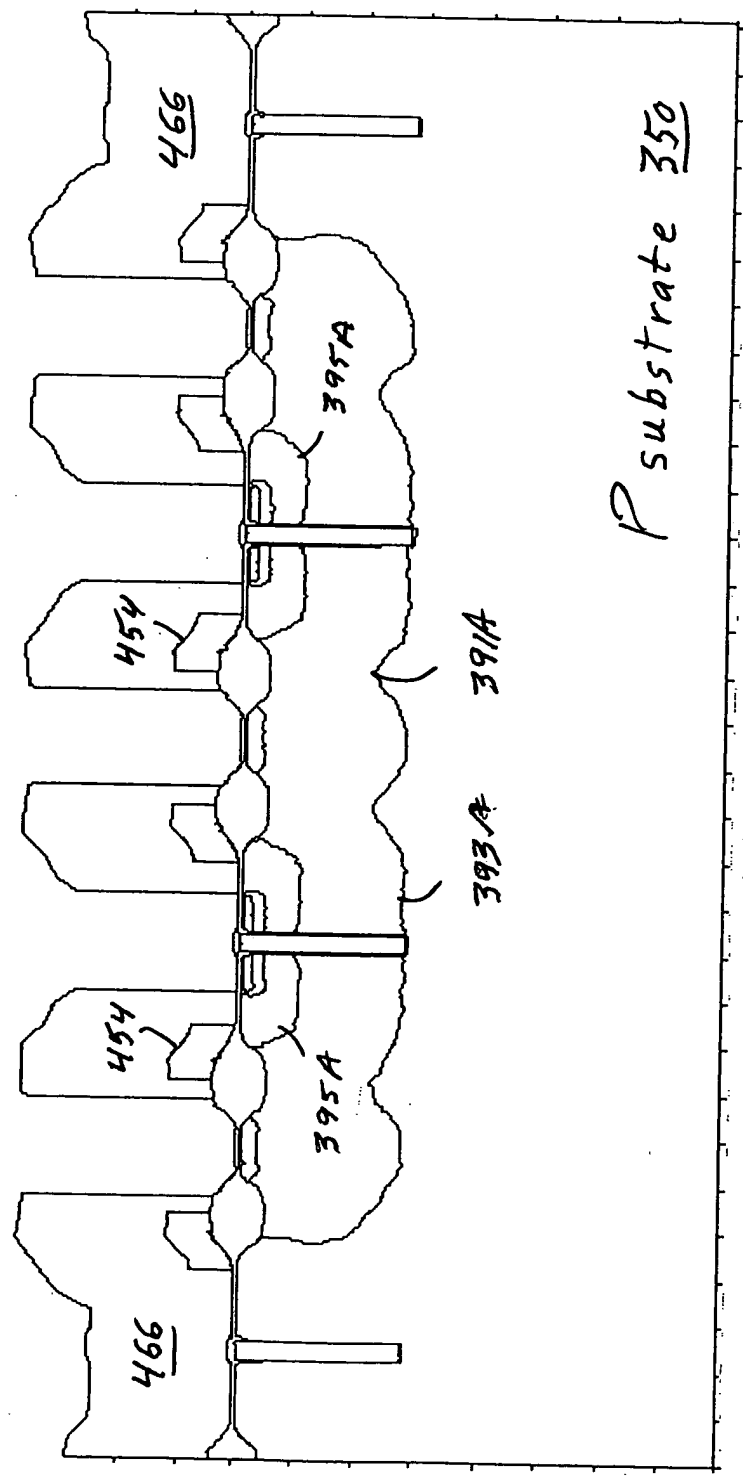


5V N-LDD Implant

Fig 60C

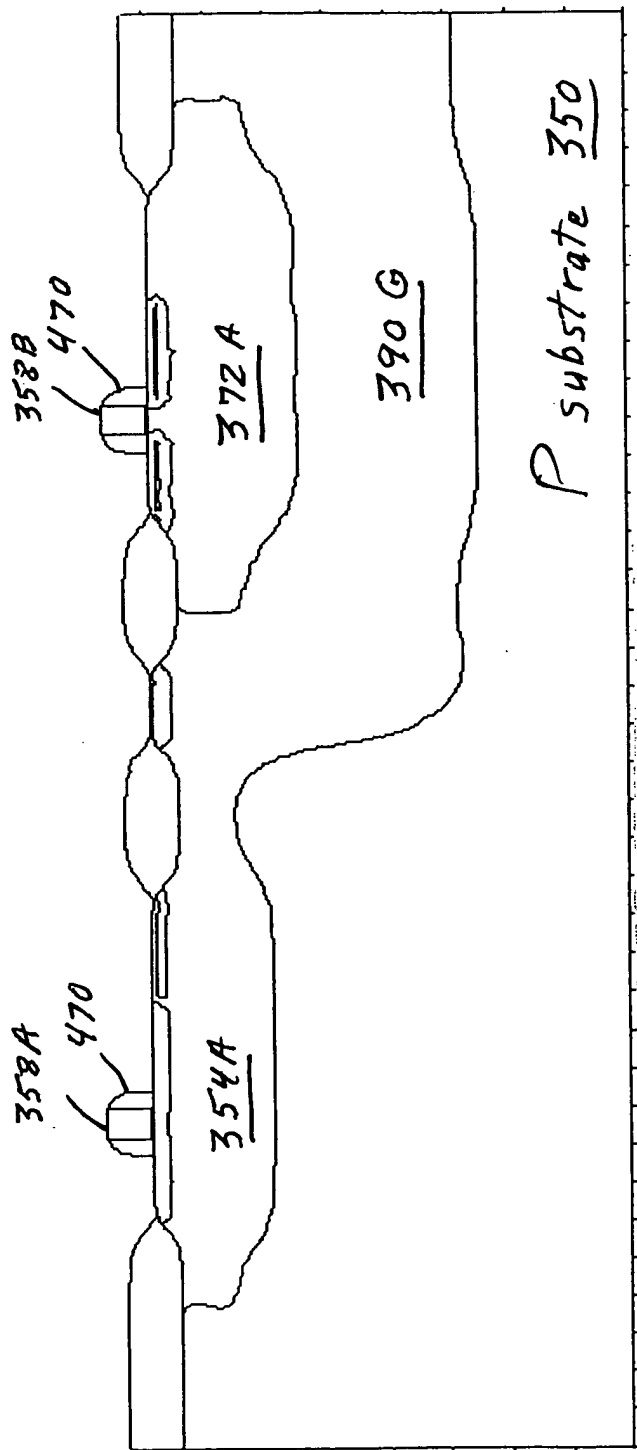
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30V Lateral Trench DMOS 308



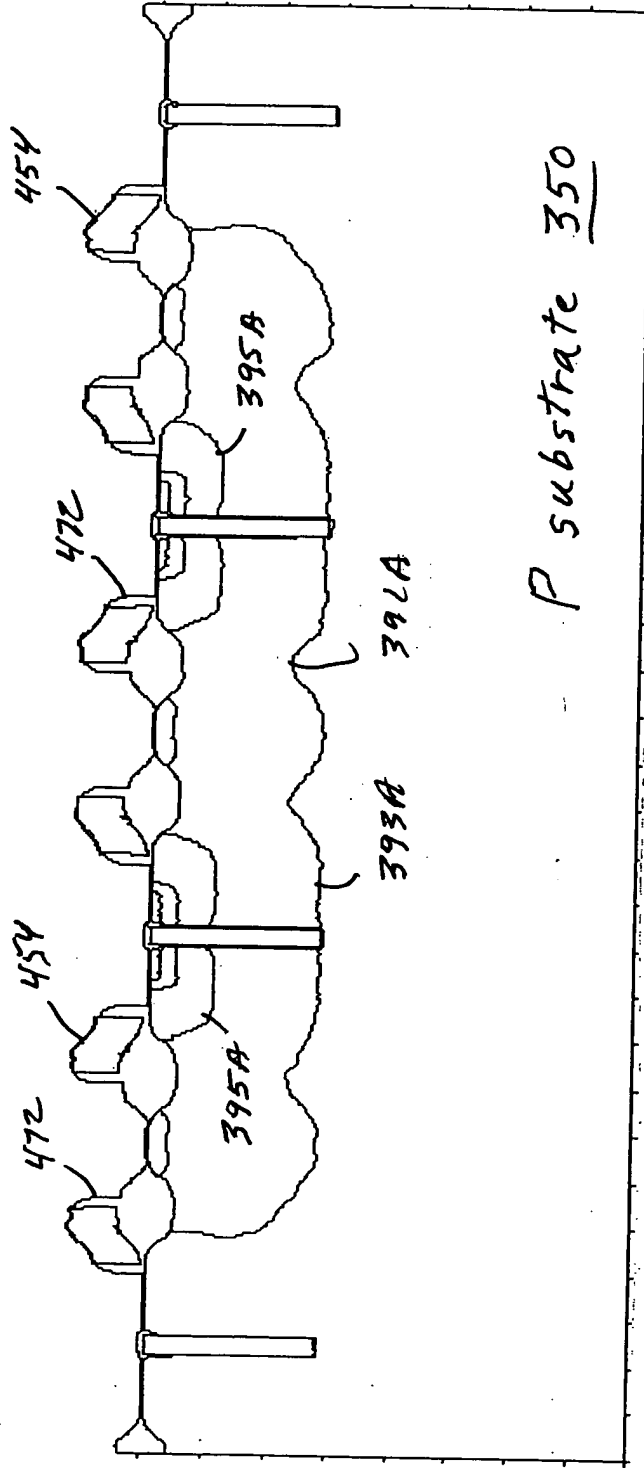
5V N-LDD Implant  
Fig. 60D

5V PMOS 301      5V NMOS 302



Sidewall Spacers  
Fig. 61A

# 30V Lateral Trench DMOS 308

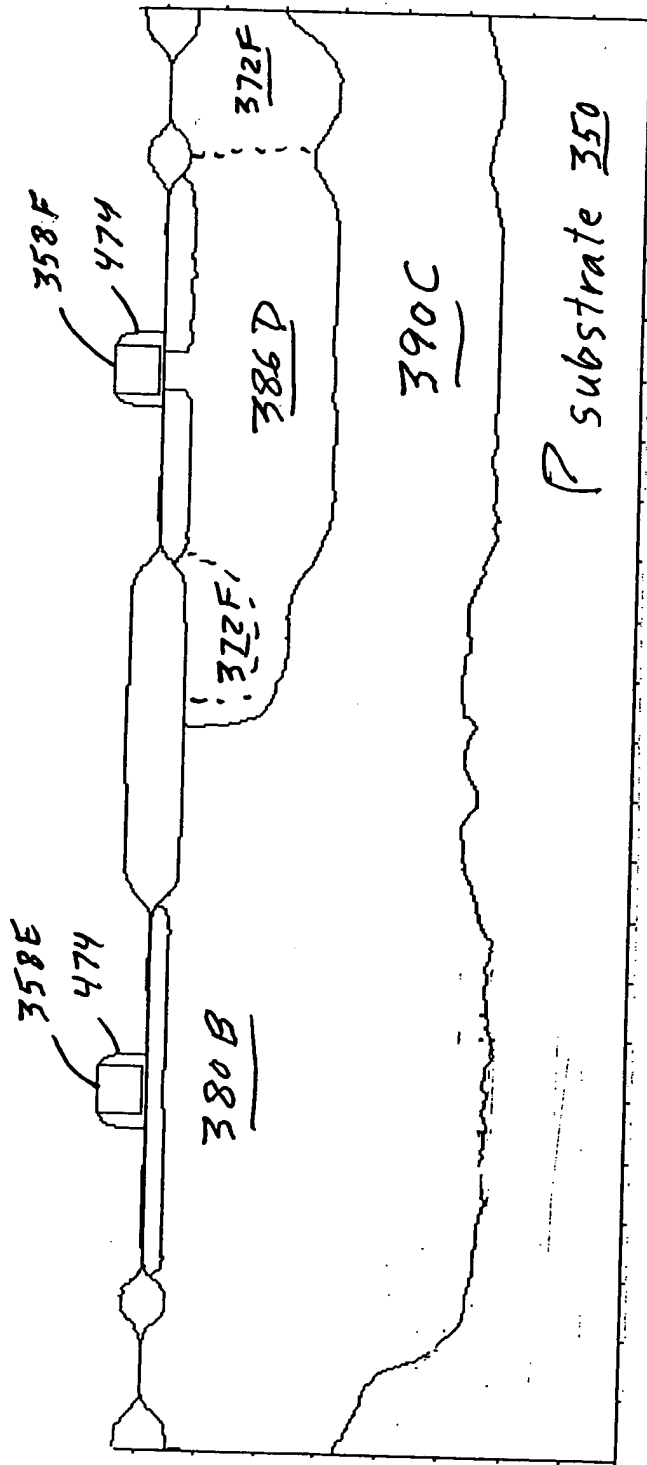


P substrate 350

Side wall Spacers

Fig. 61D

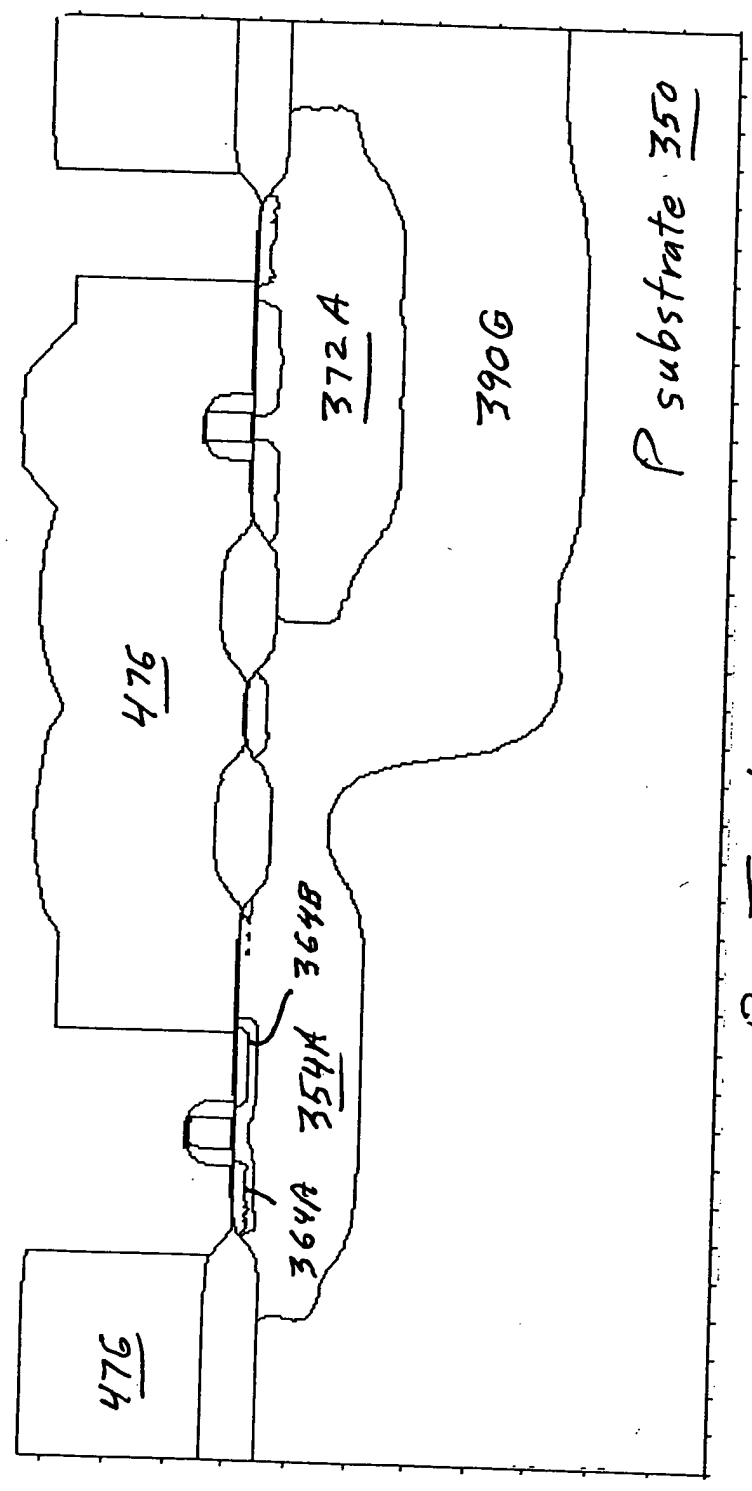
Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



Sidewall Spacers  
Fig. 61E



5V PMOS 301      5V NMOS 302

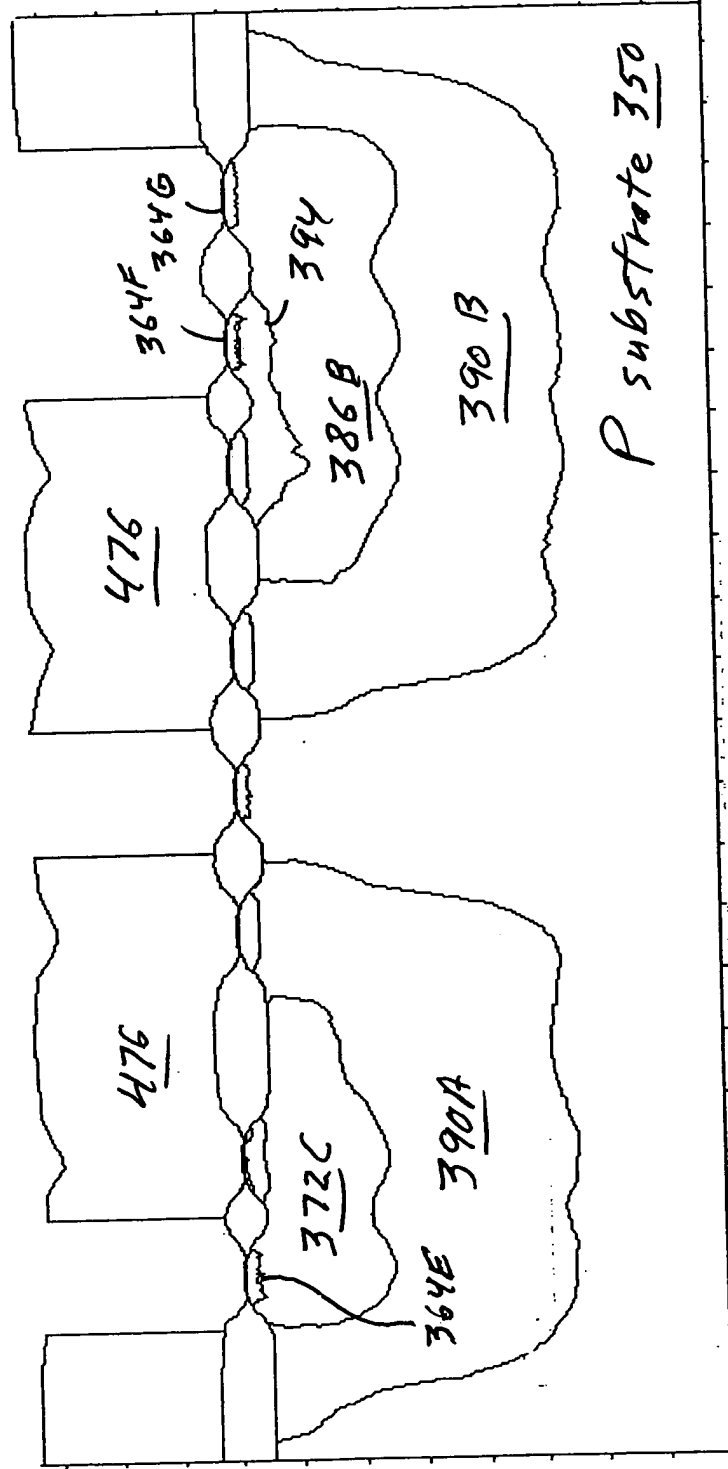


Pt Implant  
Fig. 62A

# High F<sub>r</sub> Layout

5V PNP 306

5V NPN 305

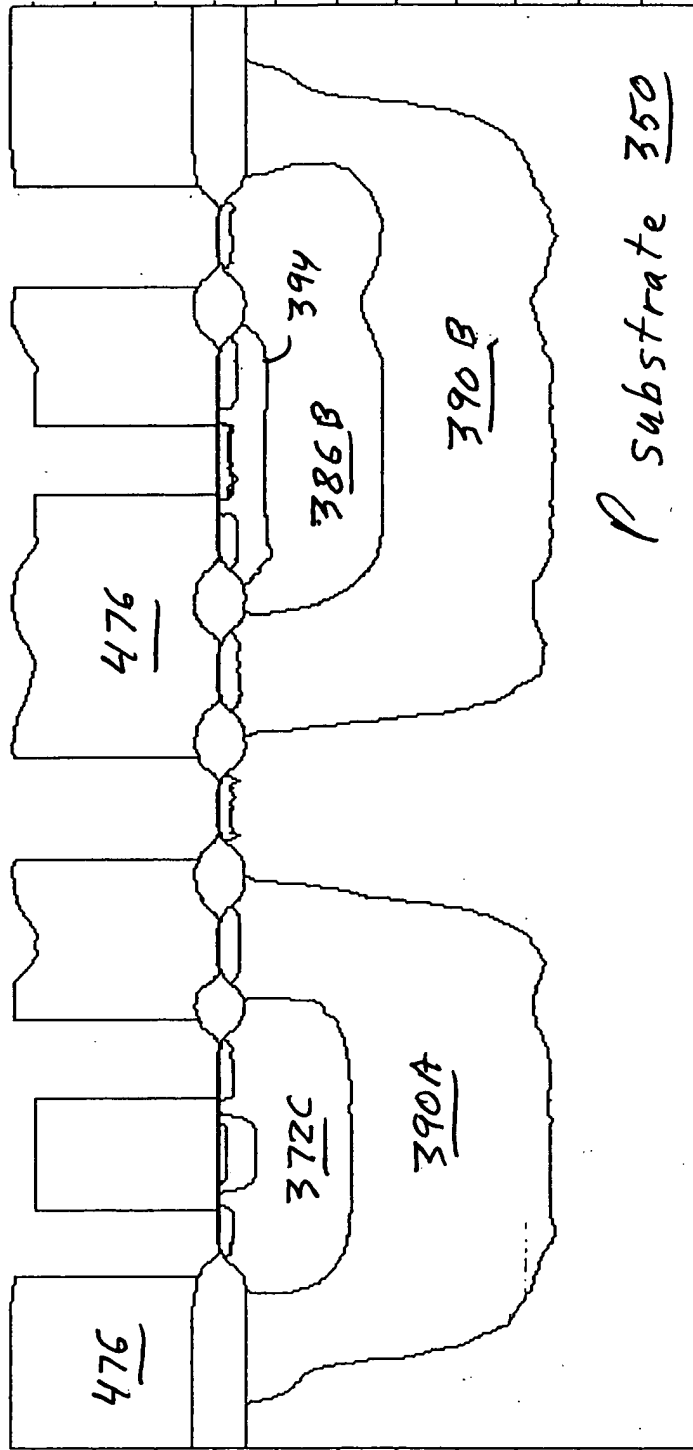


P+ Implant  
Fig. 62B

Conventional Layout

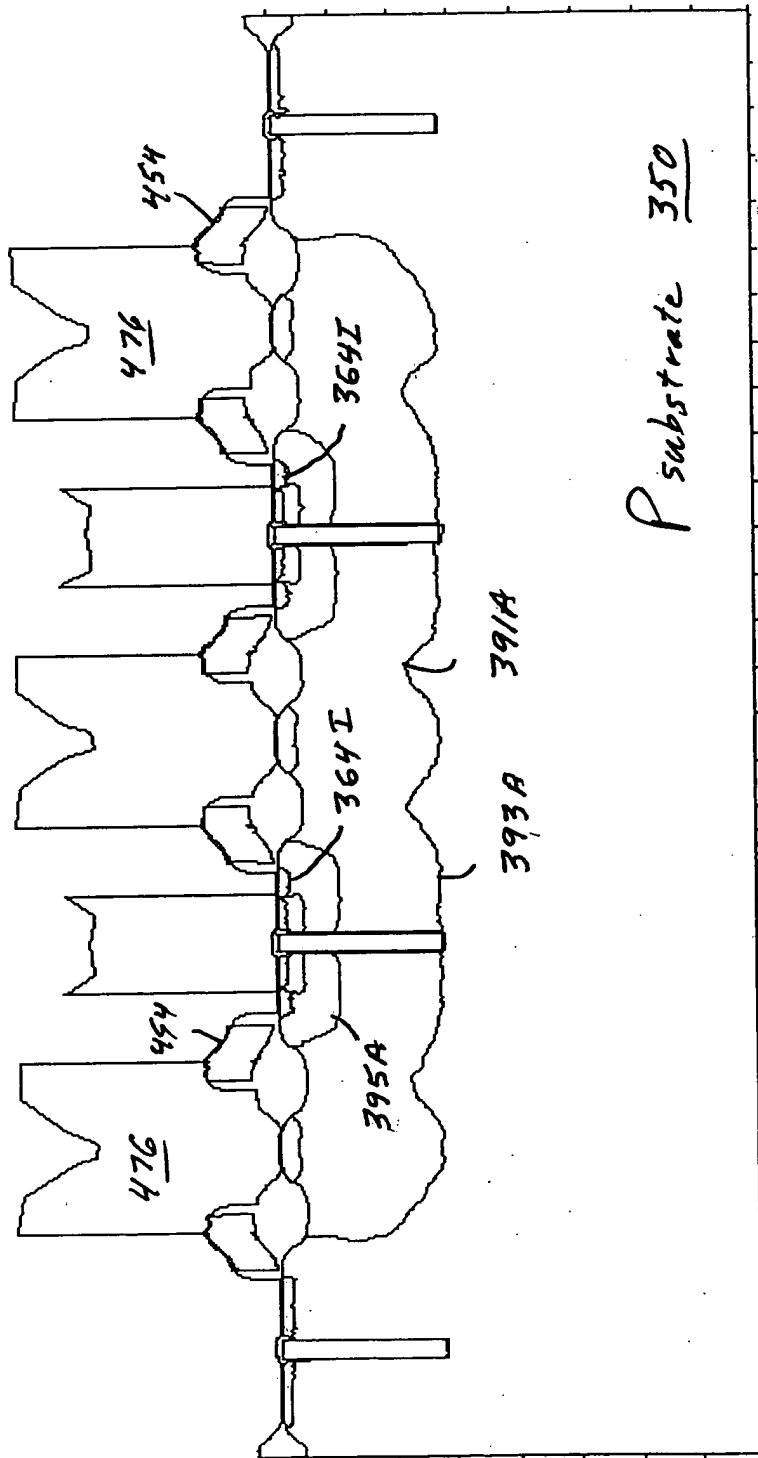
5V NPN

5 PNP



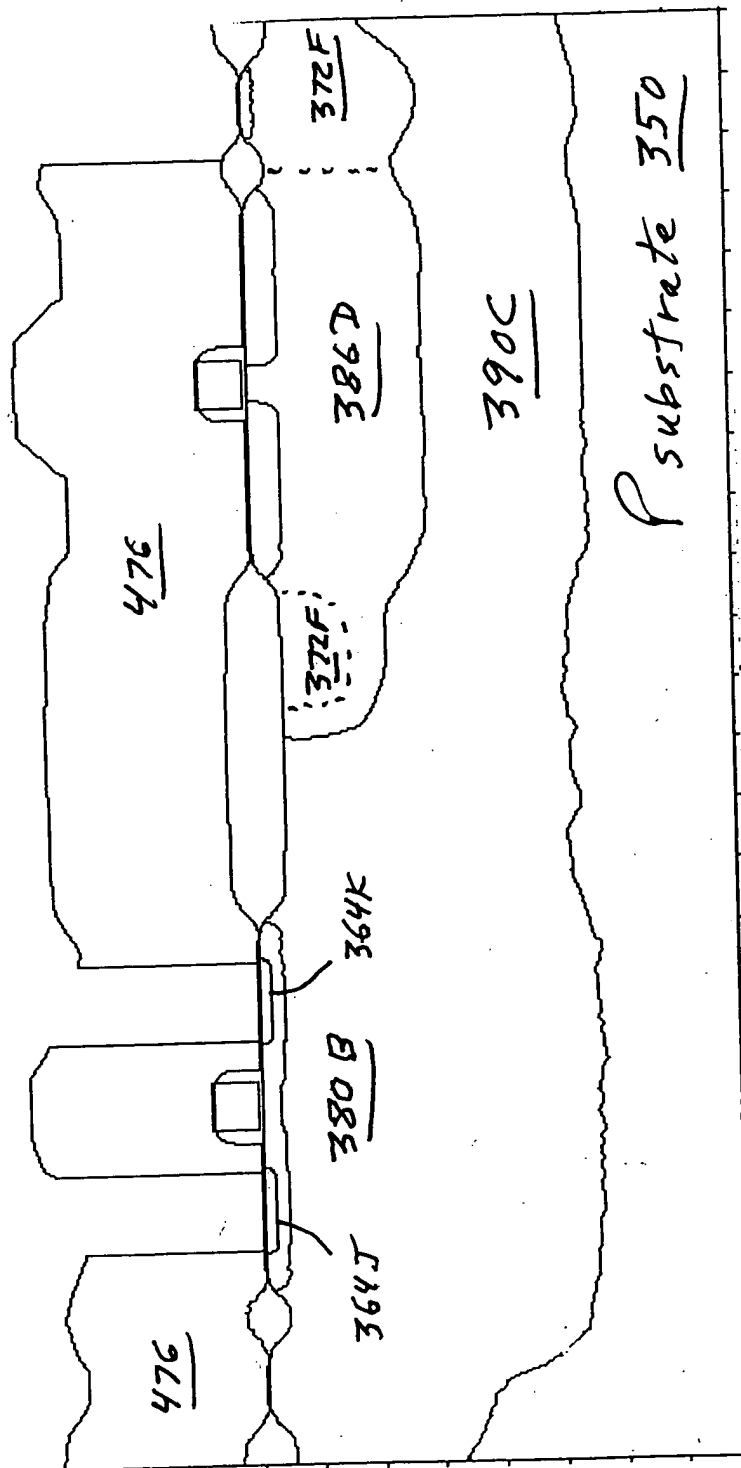
Pt Implant  
Fig. 62C

30V Lateral Trench DMOS 308



Pt Implant  
Fig. 62D

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



Pt Implant  
Fig 62E

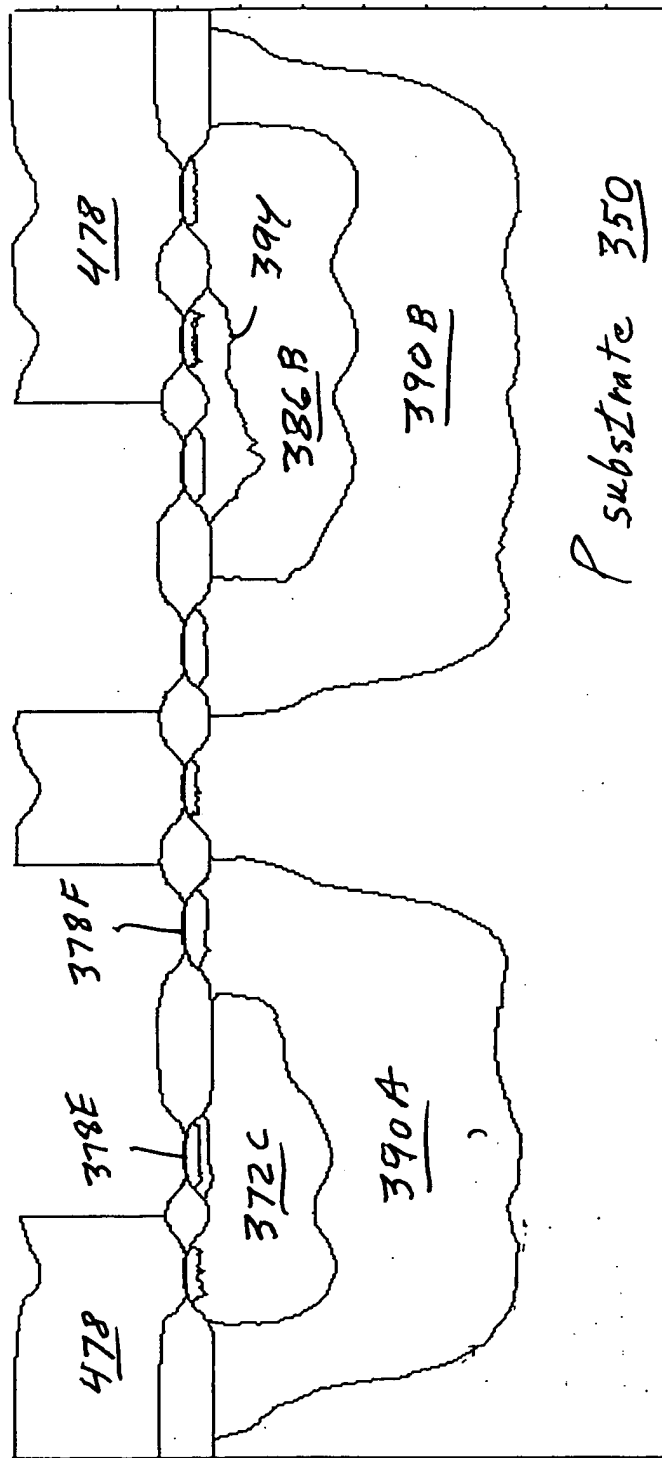
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High  $F_T$  Layout

5V NPN 305

5V PNP 306



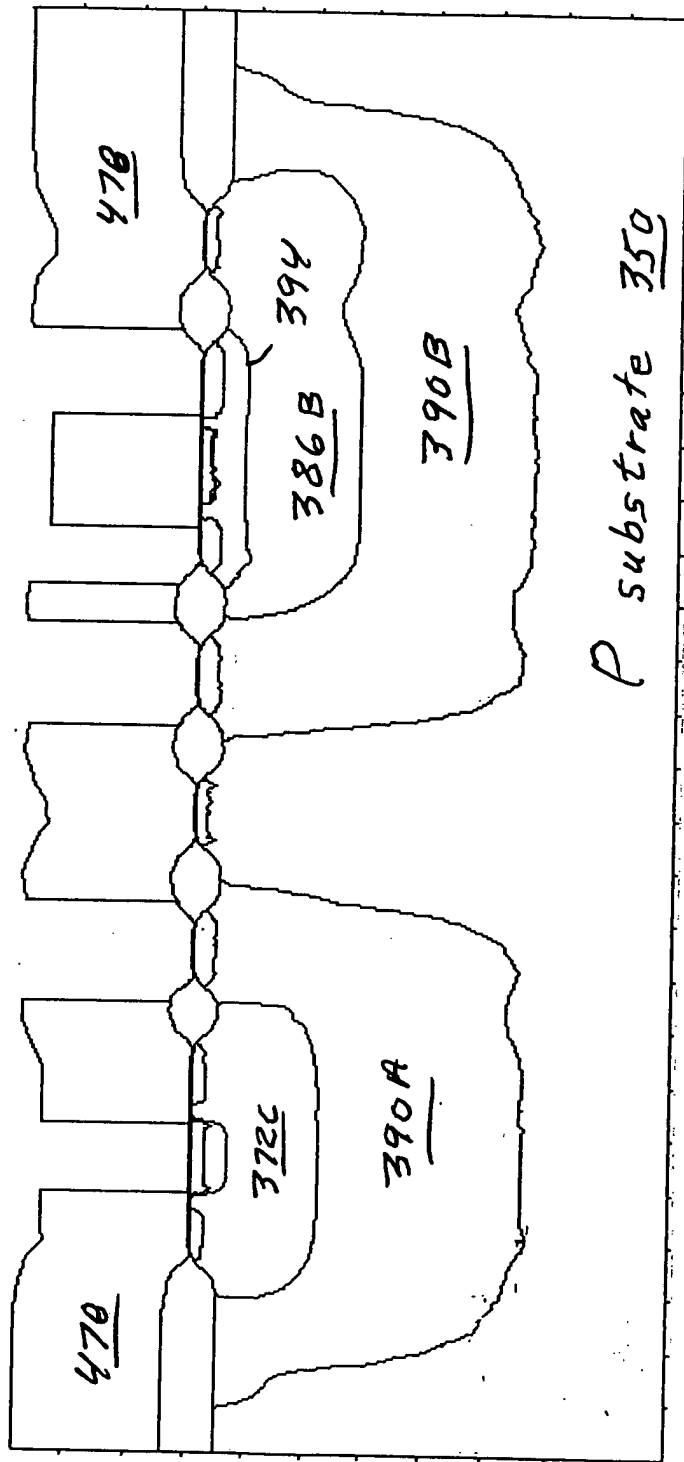
N+ Implant

Fig. 63B

Conventional Layout

5V NPN

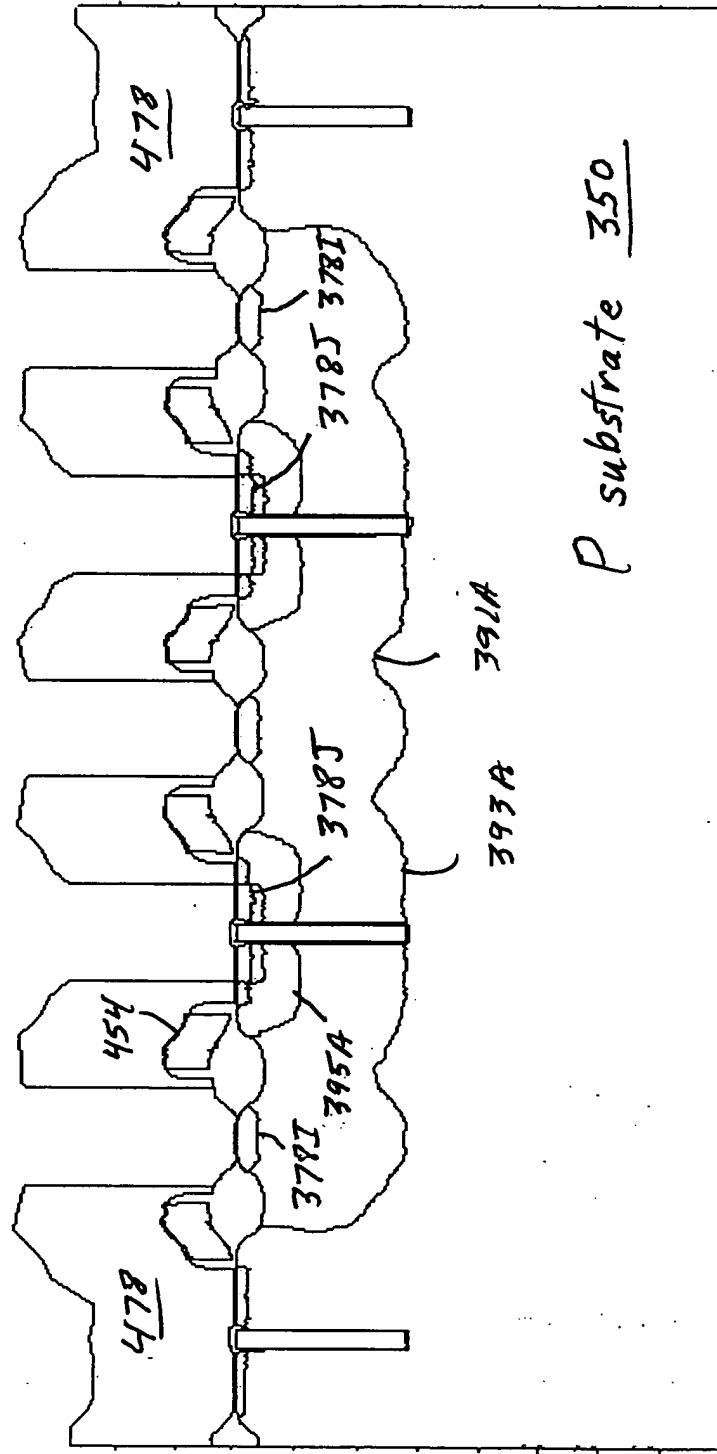
5V PNP



Nt Implant  
Fig. 63C

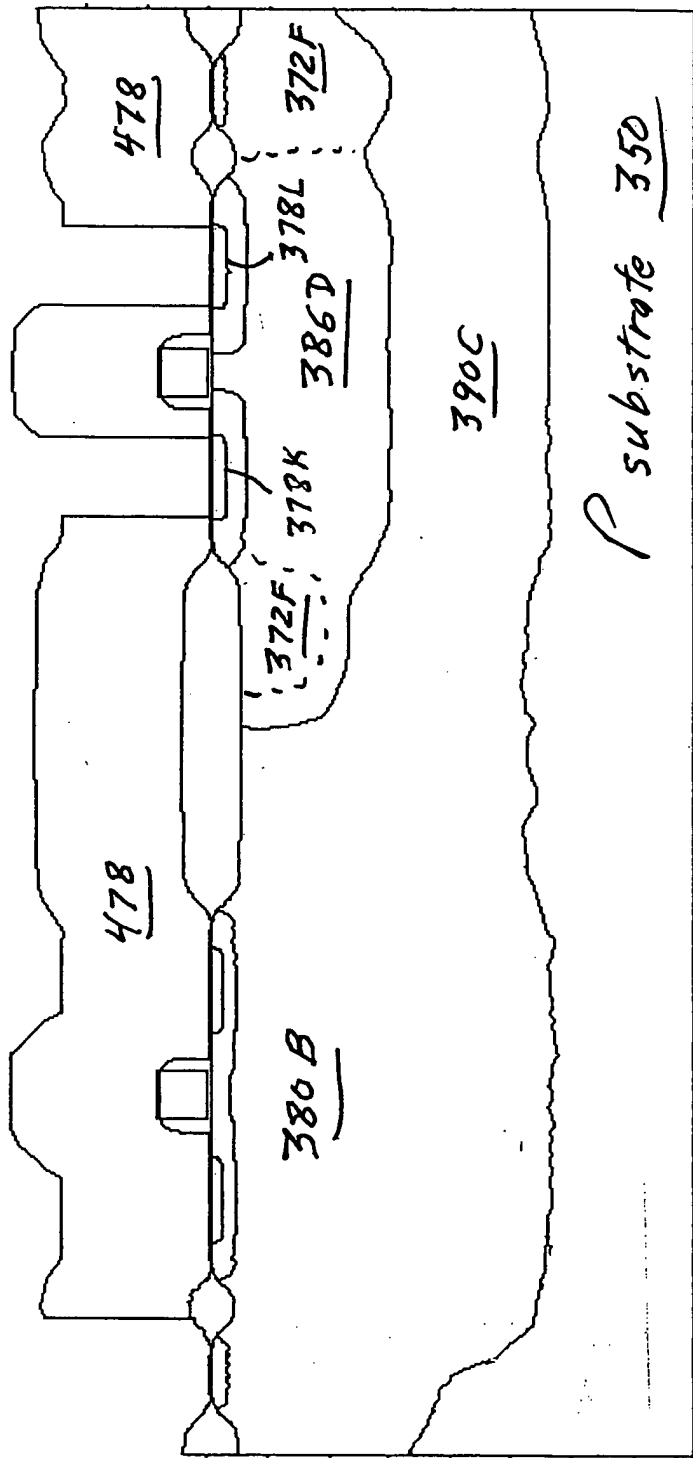


30V Lateral Trench DMOS 308

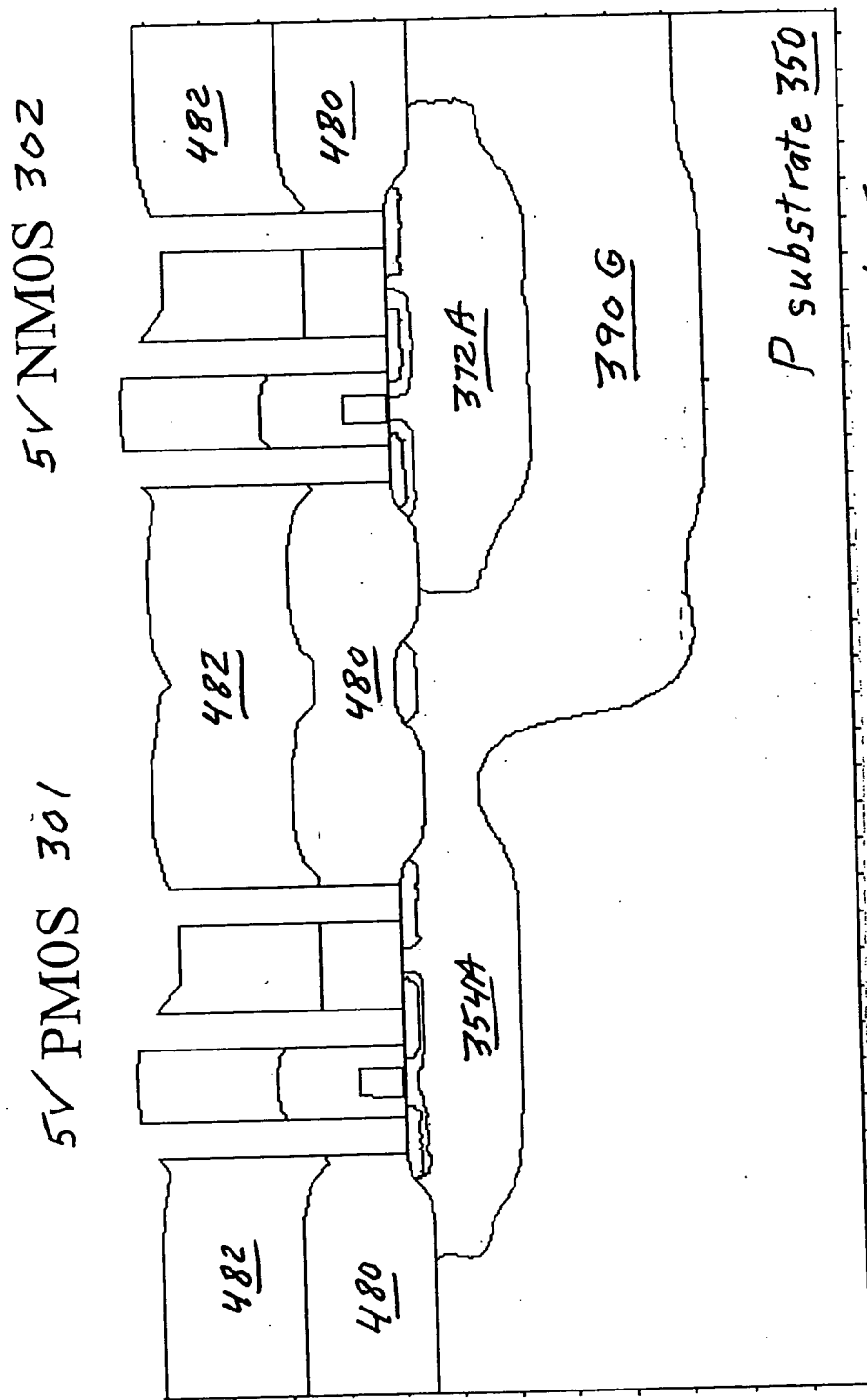


N+ Implant  
Fig 63D

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



N+ Implant  
Fig 63E

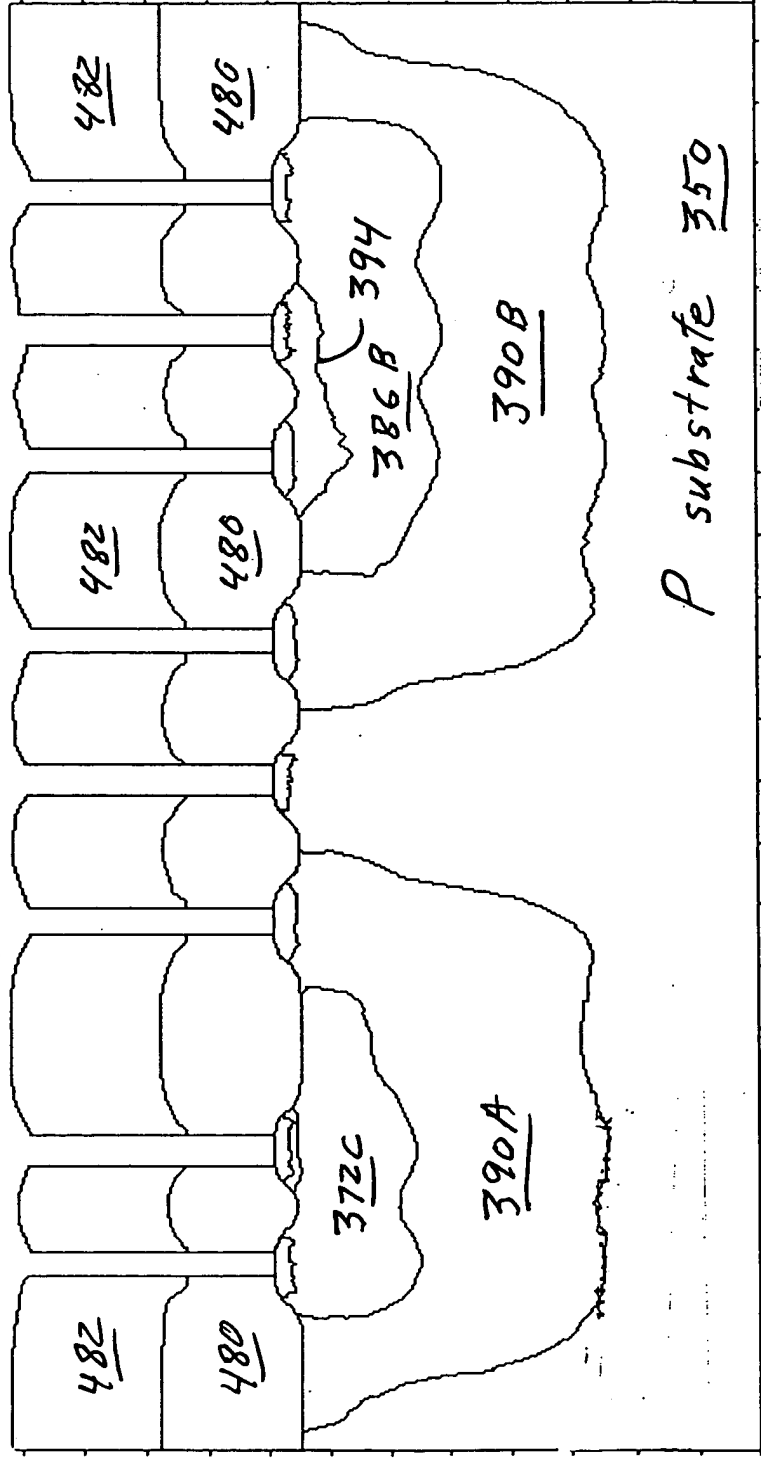


Interlayer Dielectric Deposition and Etch  
Fig. 64A

High  $F_T$  Layout

5V NPN 305

5V NPN 306



Interlayer Dielectric Deposition and Etch

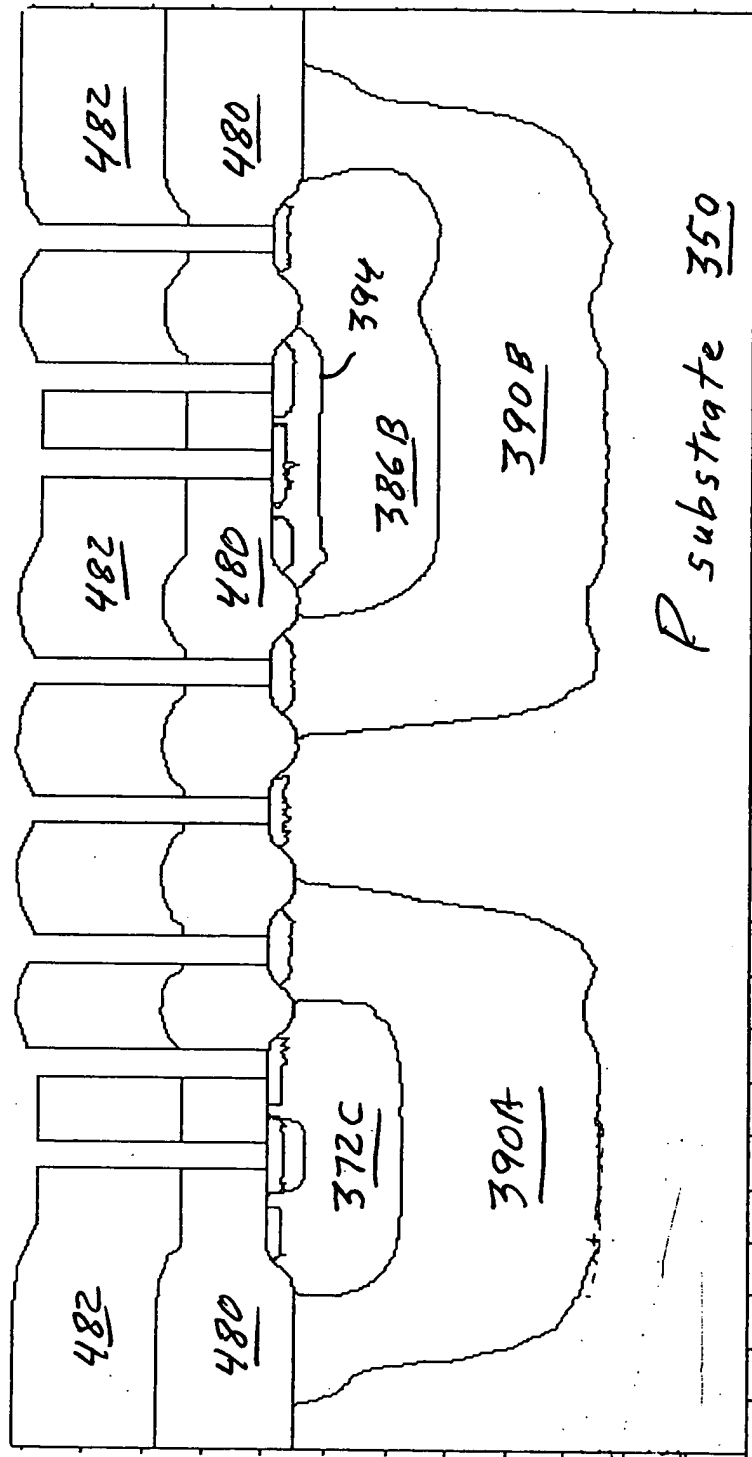
Fig. 64B

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Conventional Layout

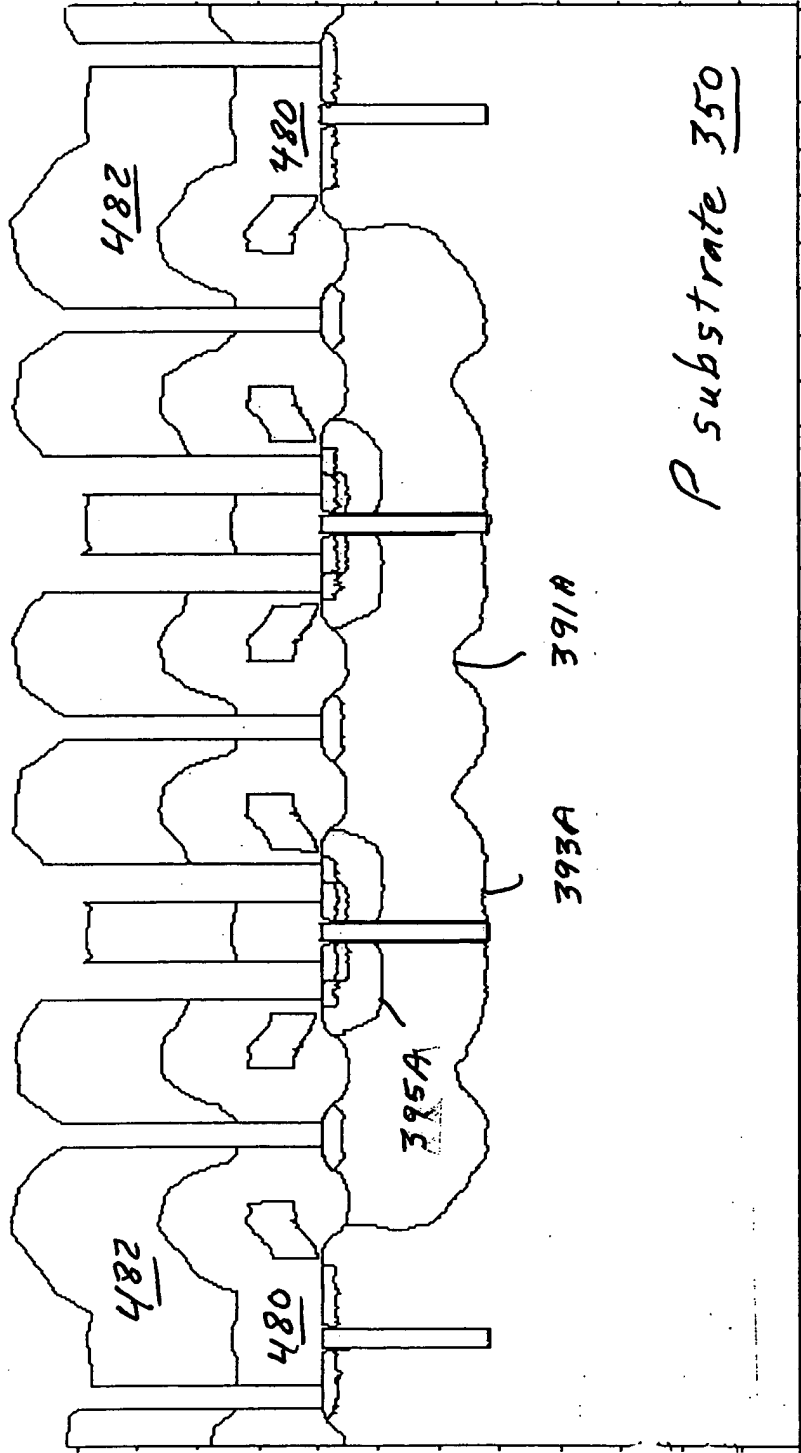
5V NPN

5V PNP



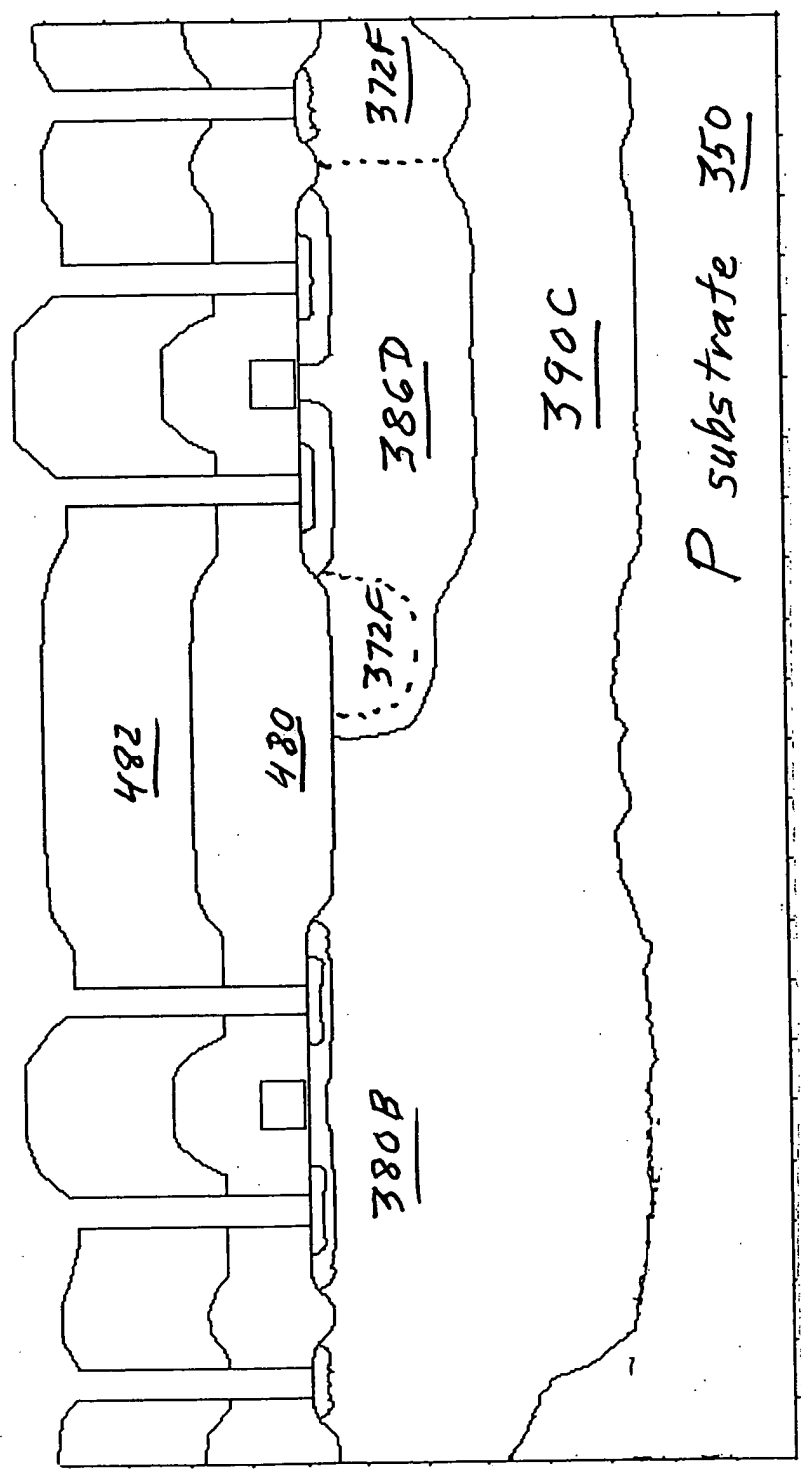
Interlayer Dielectric Deposition and Etch  
Fig. 64C

# 30V Lateral Trench DMOS 308



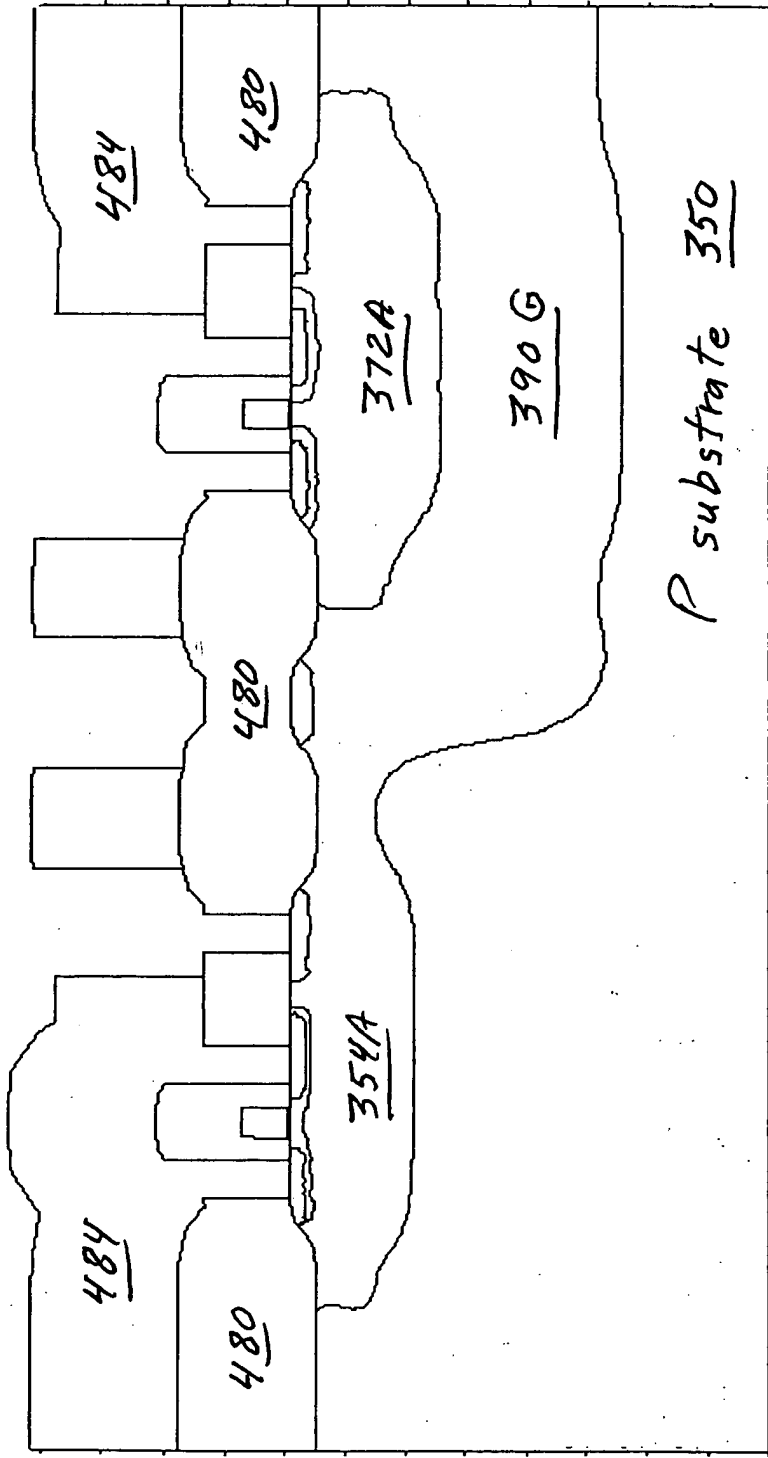
Interlayer Dielectric Deposition and Etch  
Fig. 64D

Symmetrical 12V CMOS  
12V PMOS 309      12V NMOS 310



Interlayer Dielectric Deposition and Etch  
Fig 64E

5V PMOS 301      5V NMOS 302



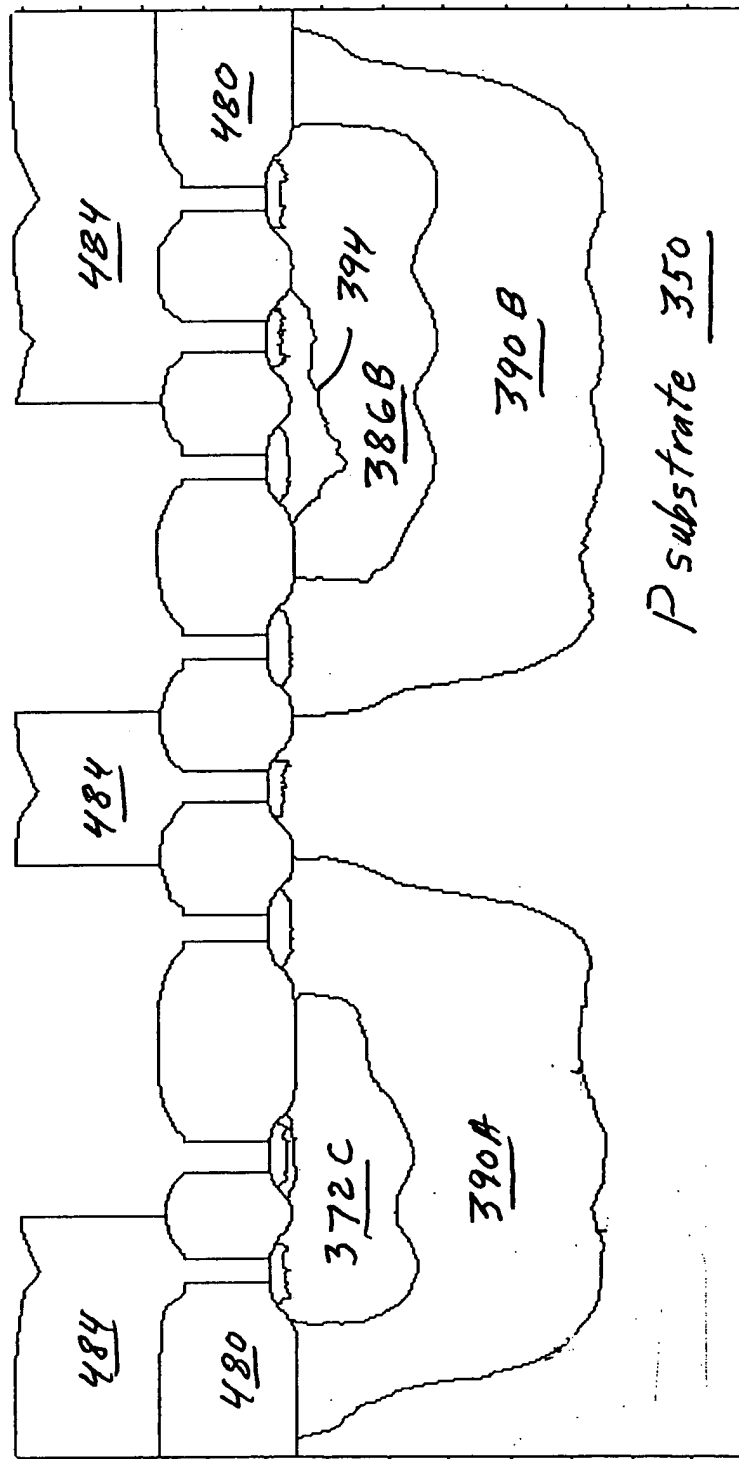
N+ plug Mask and Implant  
Fig. 65A



High F<sub>T</sub> Layout

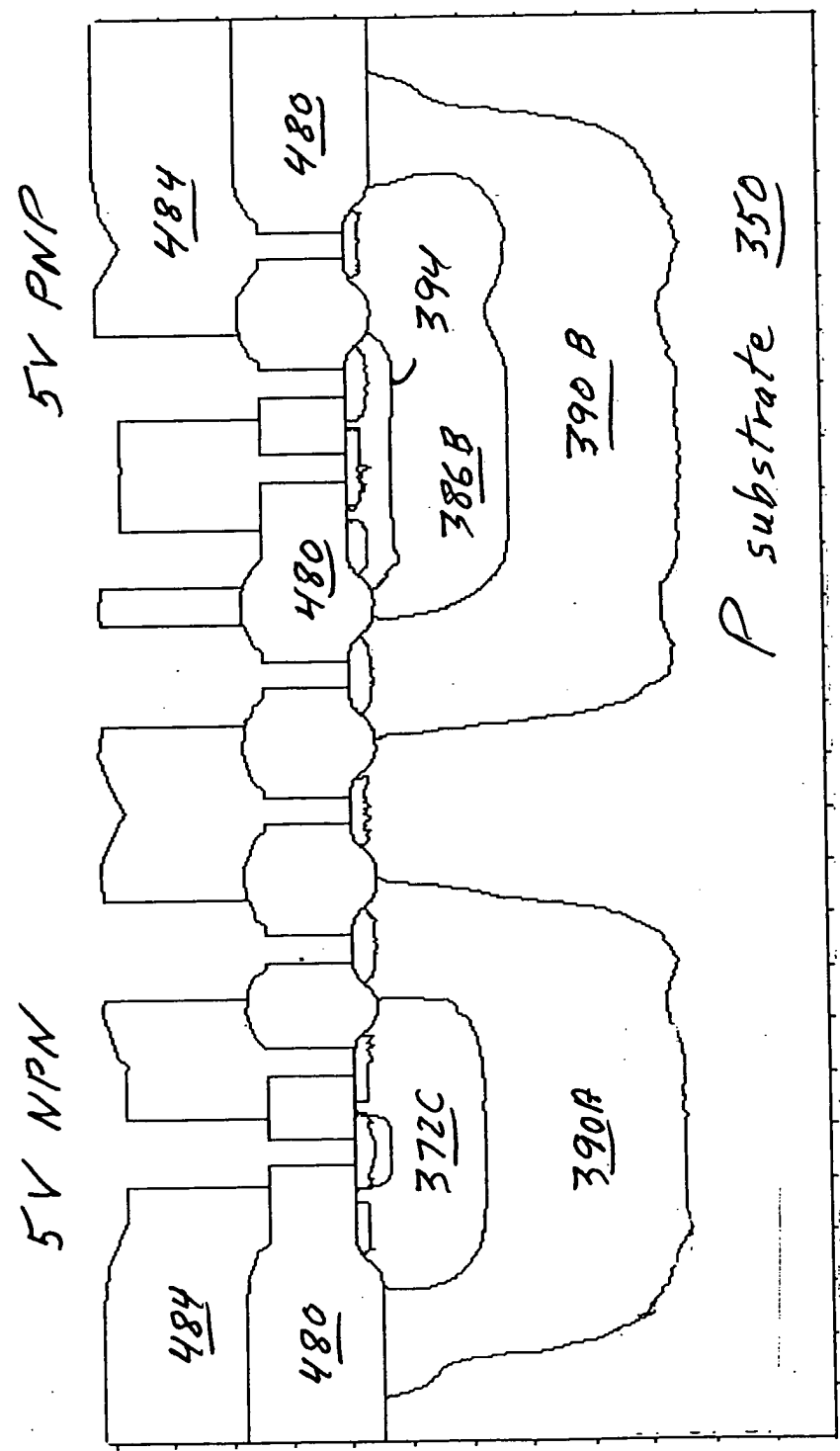
5V NPN 305

5V PNP 306



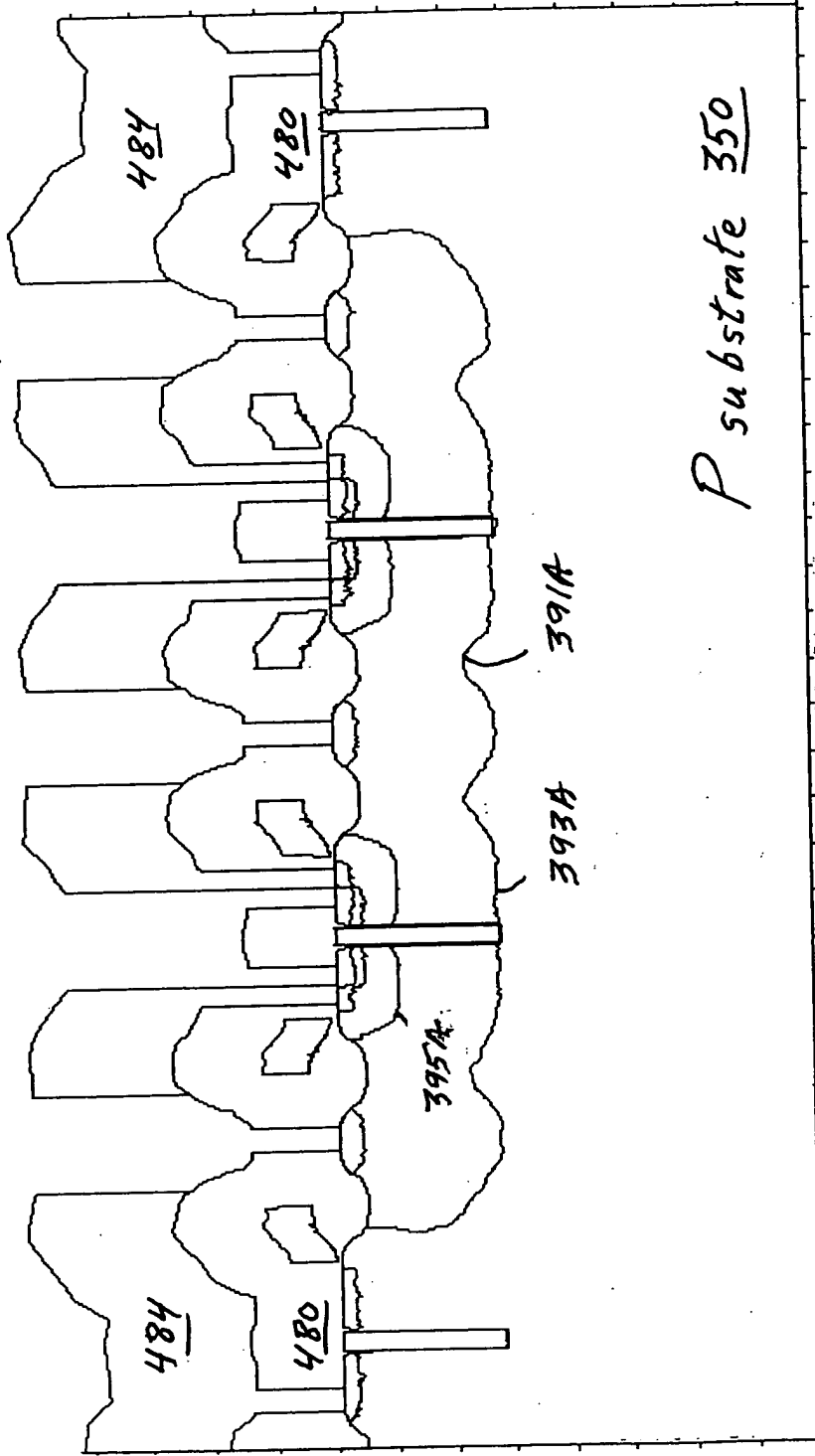
N-play Mask and Implant  
Fig 65B

Conventional Layout



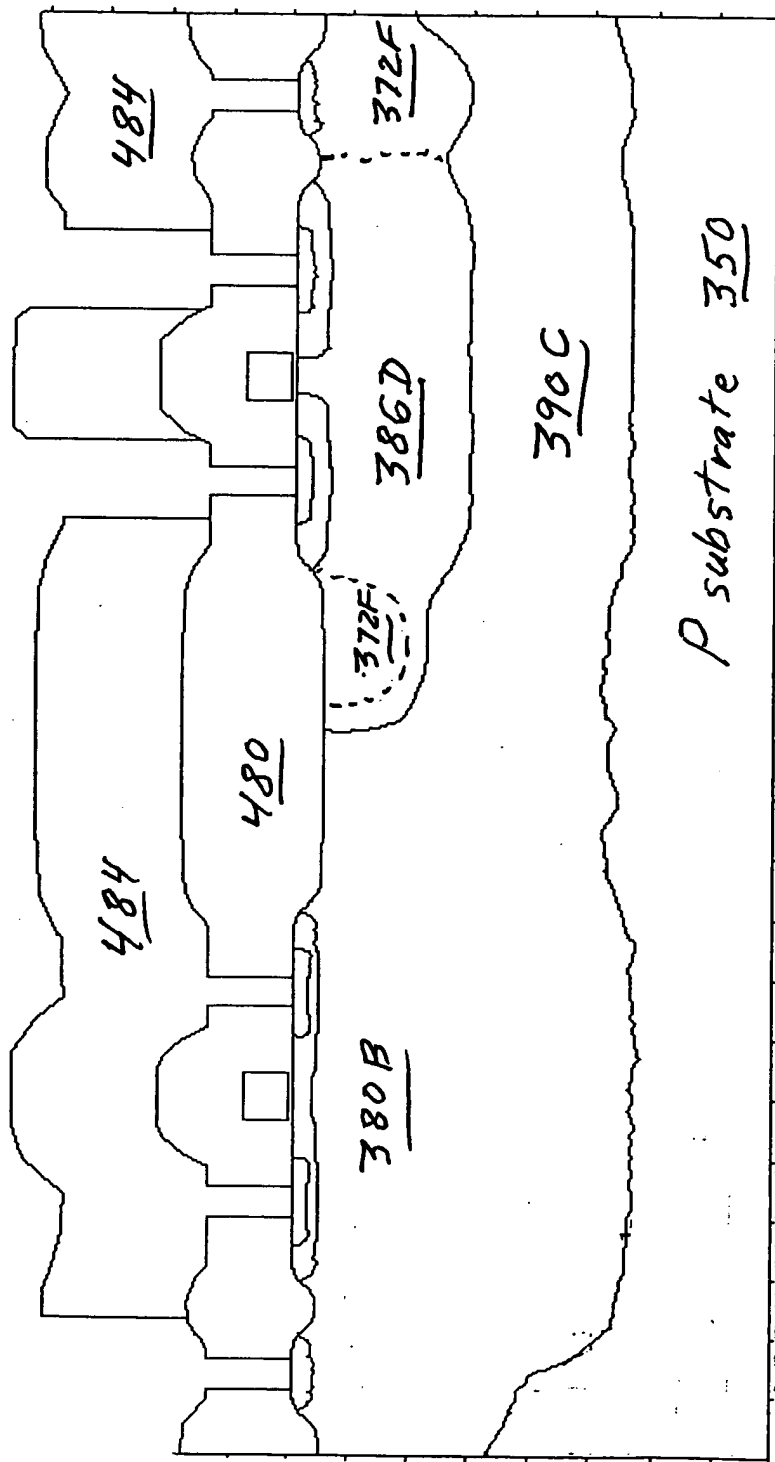
N-plug Mask and Implant  
Fig. 65C

30V Lateral Trench DMOS 308



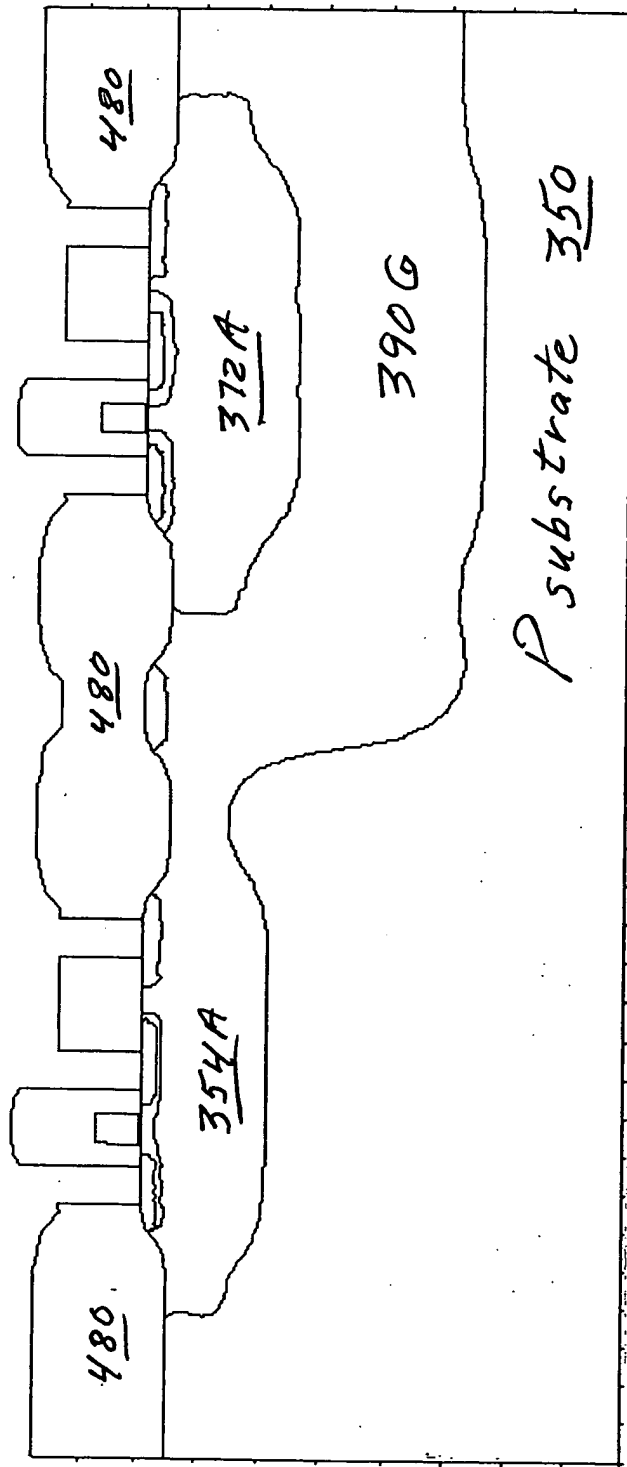
N+ plug Mask and Implant  
Fig 65D

Symmetrical 12V CMOS  
 12V PMOS 309      12V NMOS 310



N+plug Mask and Implant  
 Fig 65E

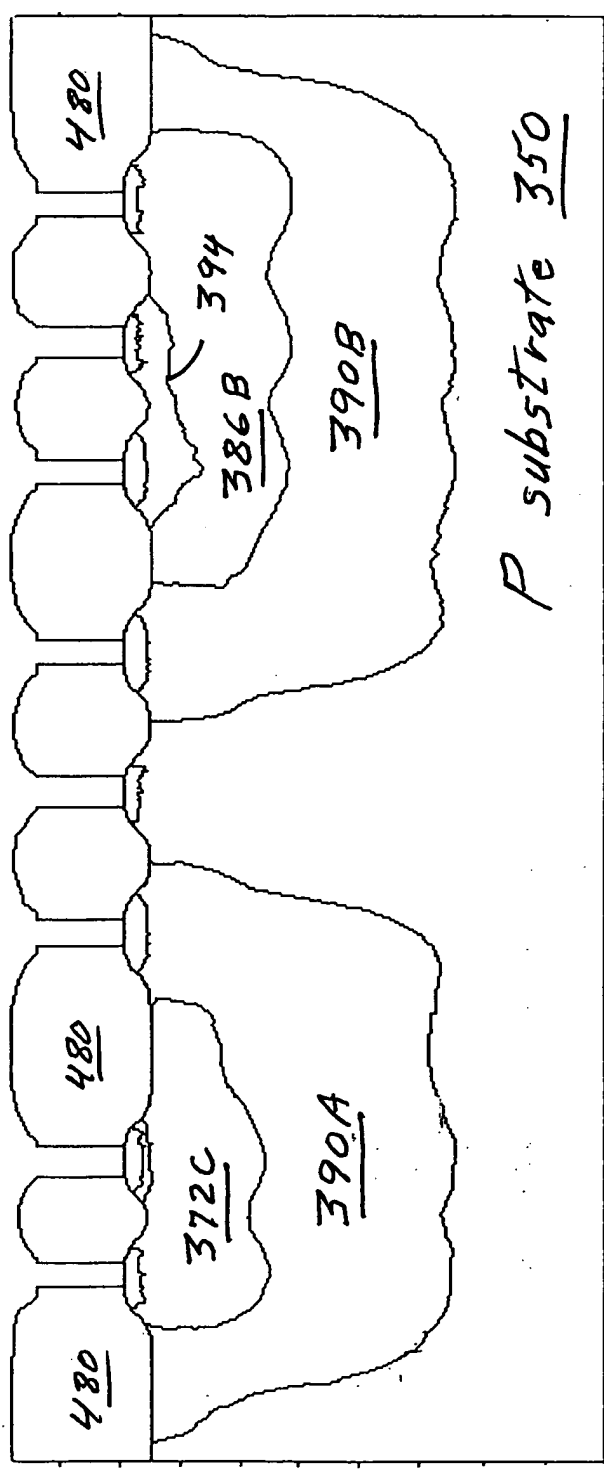
5V PMOS 301      5V NMOS 302



P-plug Implant  
Fig. 66A

High  $F_T$  Layout

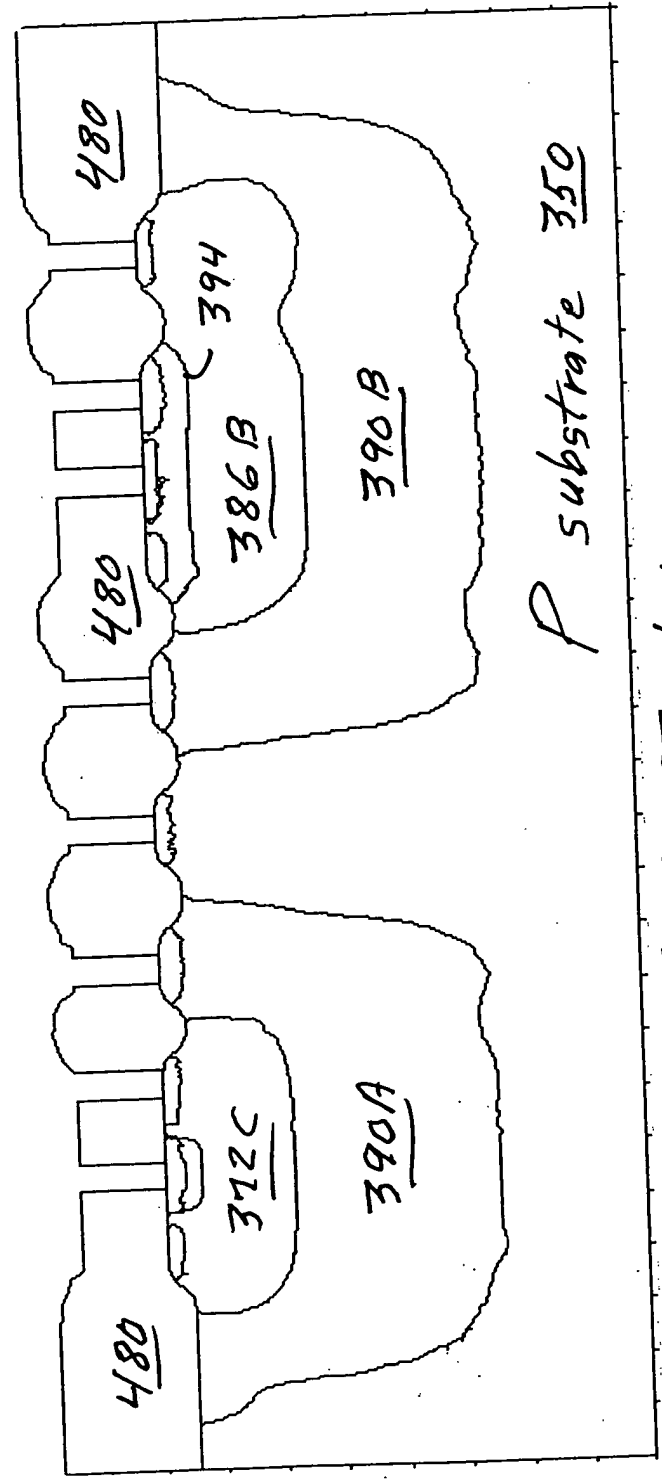
5V NPN 305      5V PNP 306



P-plug Implant  
Fig. 66B

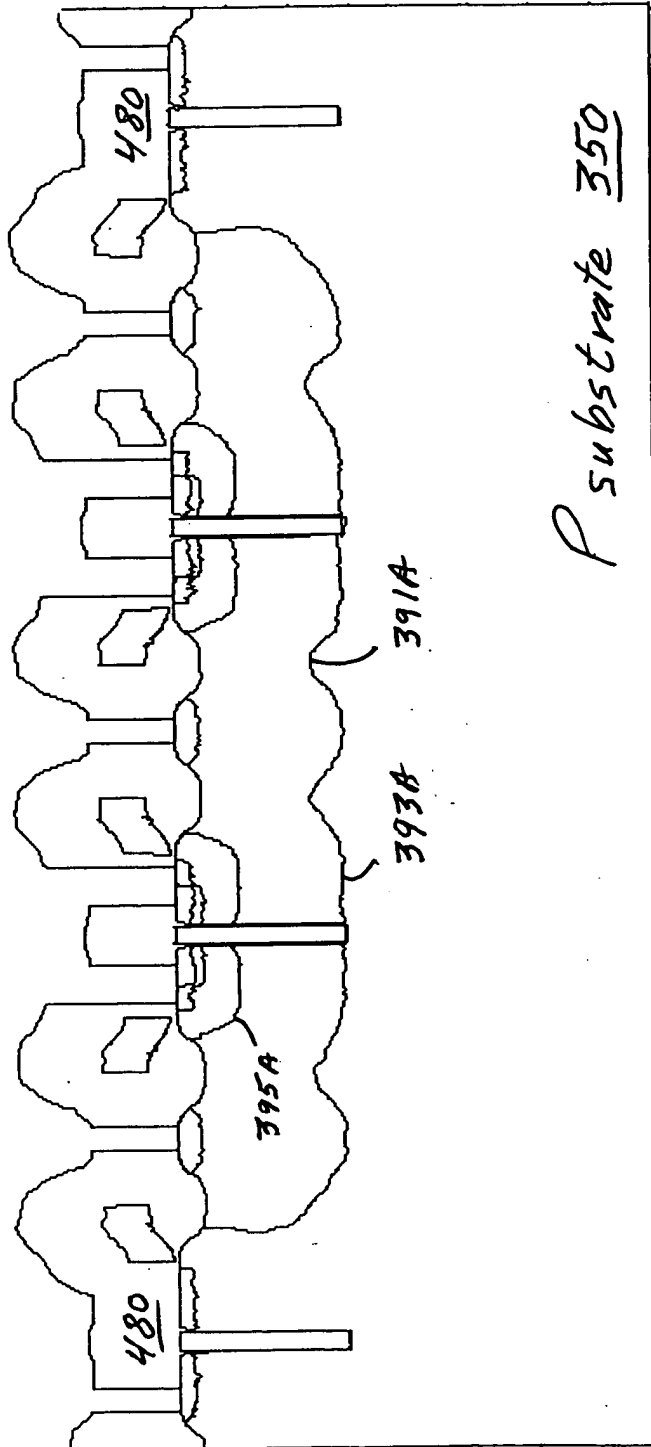
Conventional Layout

5V NPN      5V PNP



Rp lug Implant  
Fig 66C

30V Lateral Trench DMOS 308

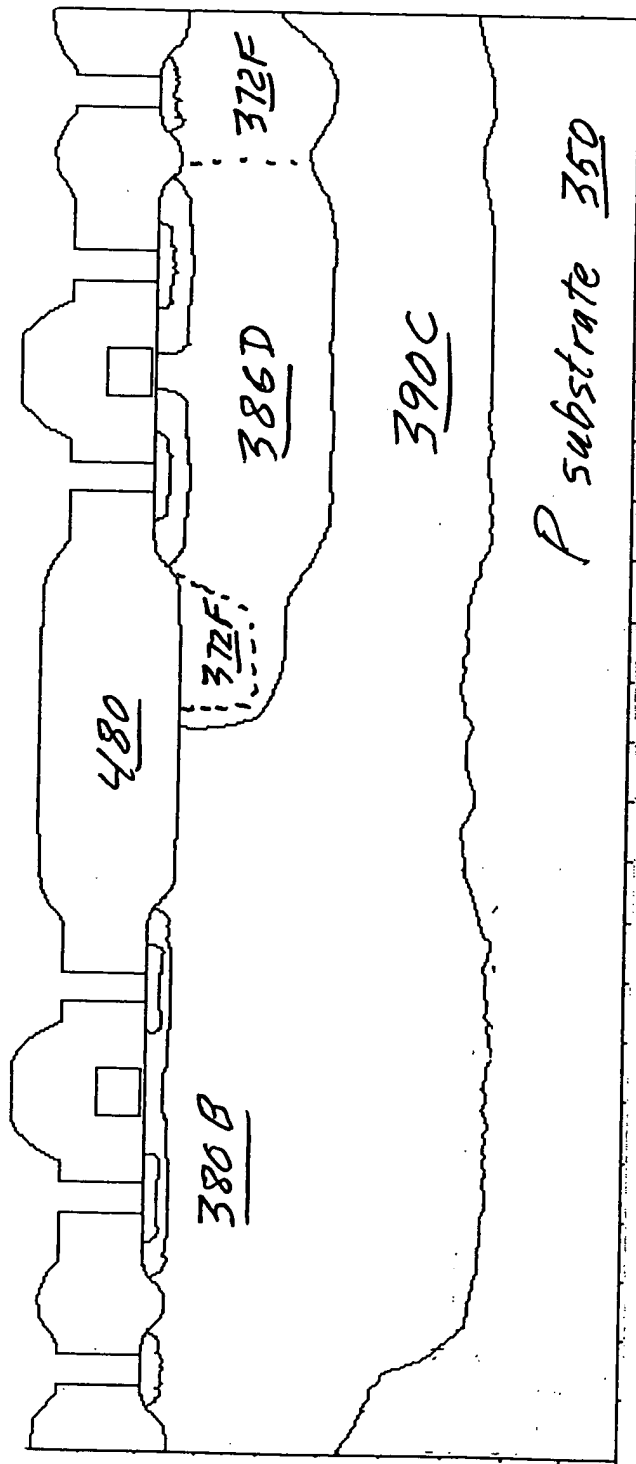


P-plug Implant  
Fig. 66D



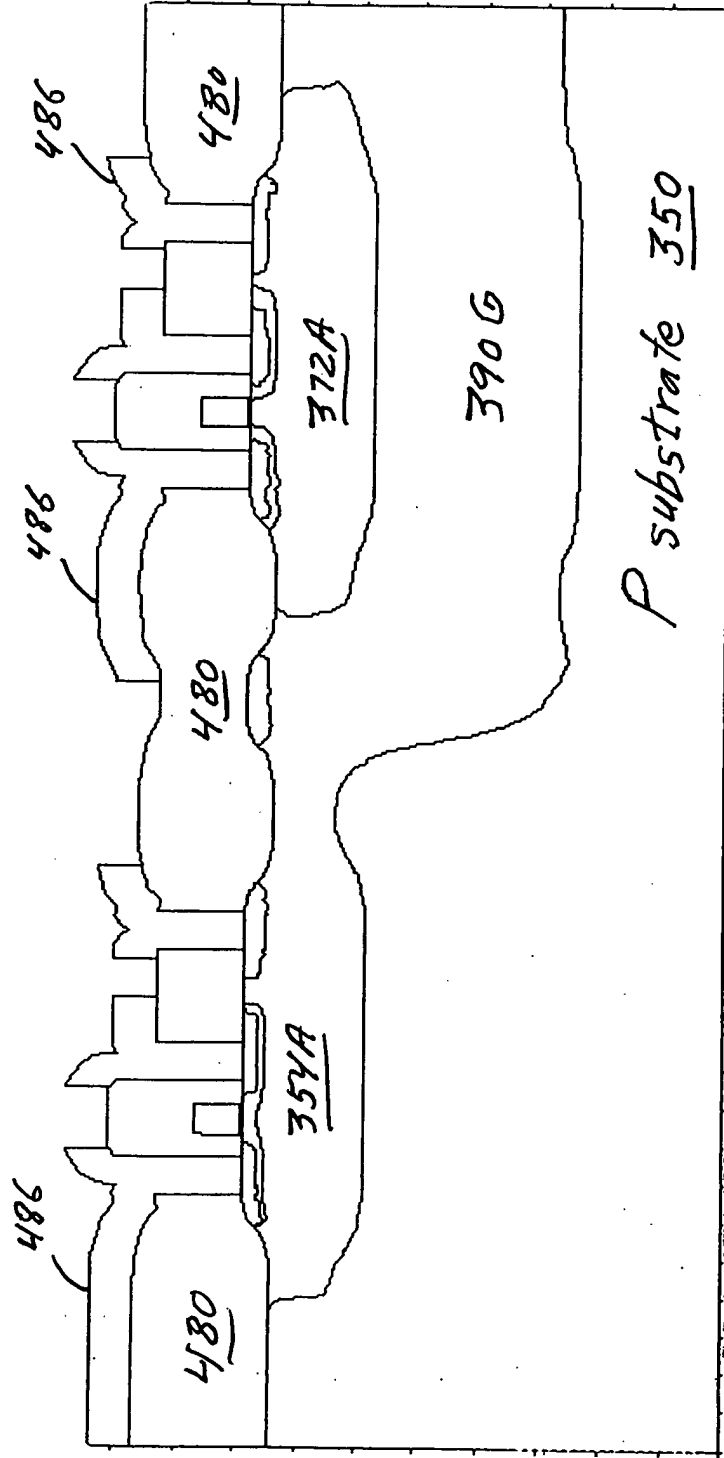
Symmetrical 12V CMOS  
 12V PMOS 309 12V NMOS 310

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P-plug Implant  
 Fig. 66E

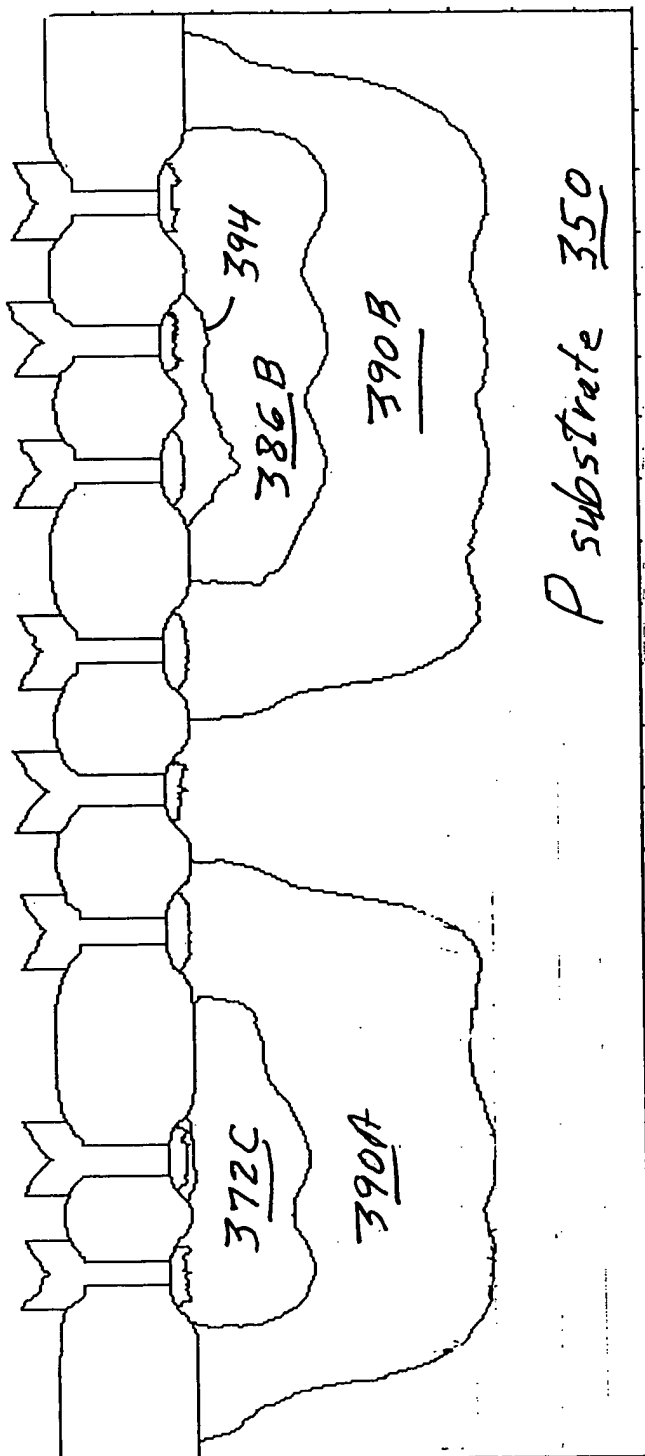
5V PMOS 301 5V NMOS 302



Metal Layer  
Fig. 67A

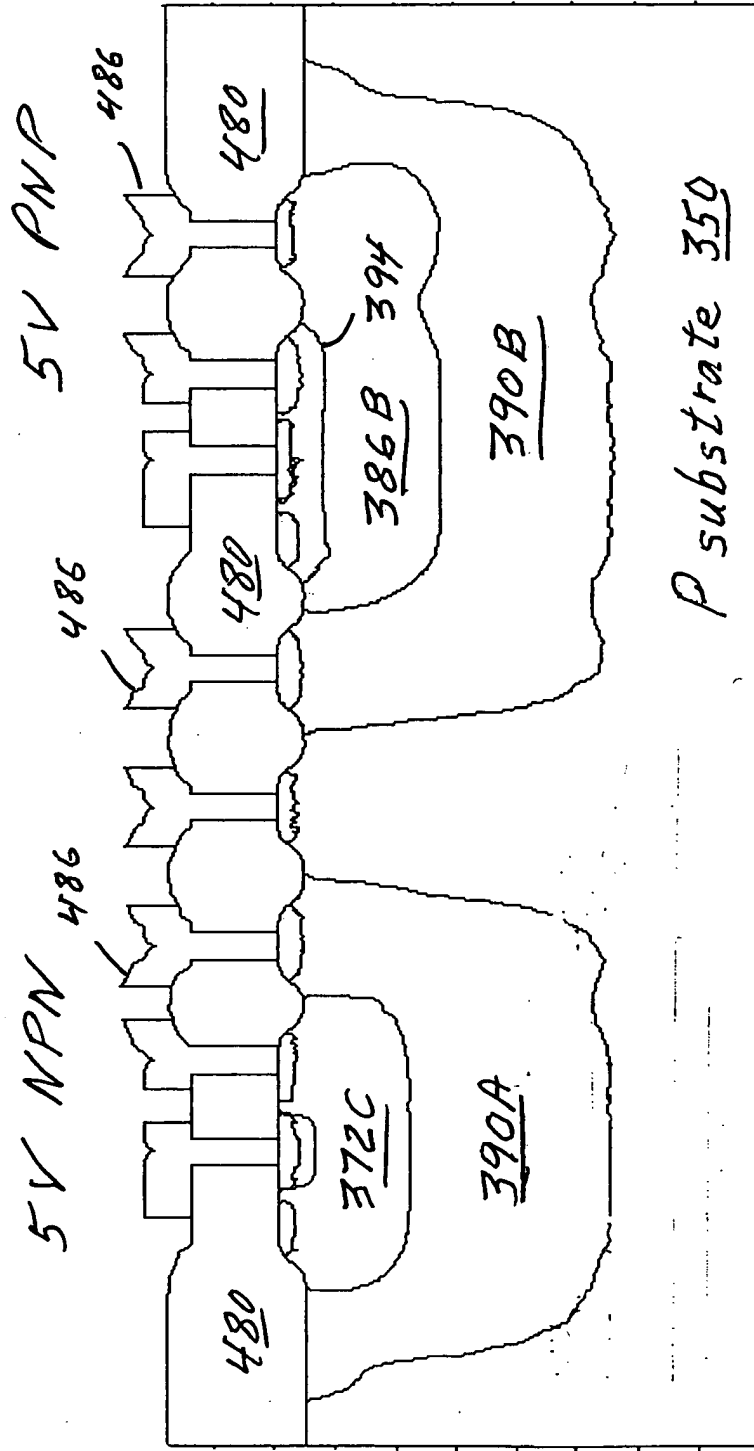
# High F<sub>T</sub> Layout

5V NPN 305      5V PNP 306



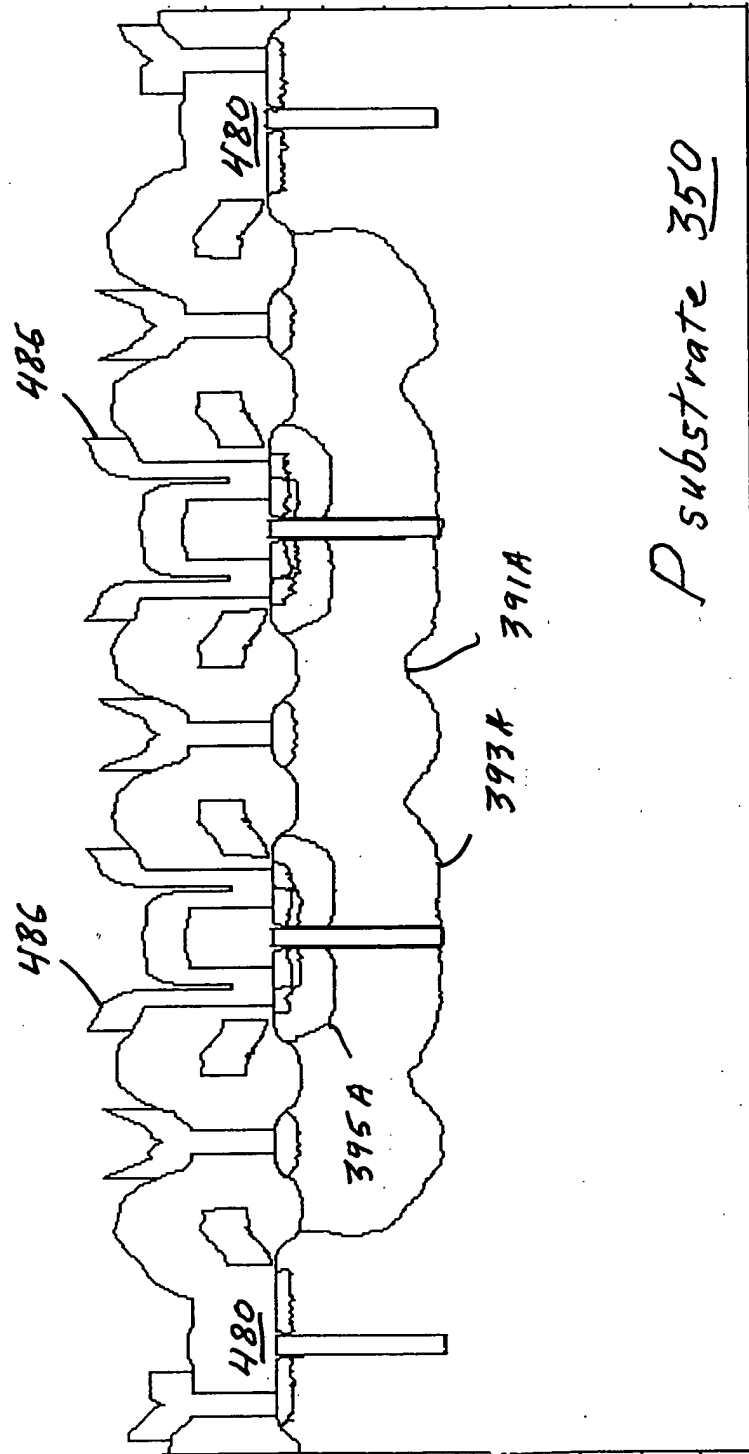
Metal Layer  
Fig. 67B

# Conventional Layout



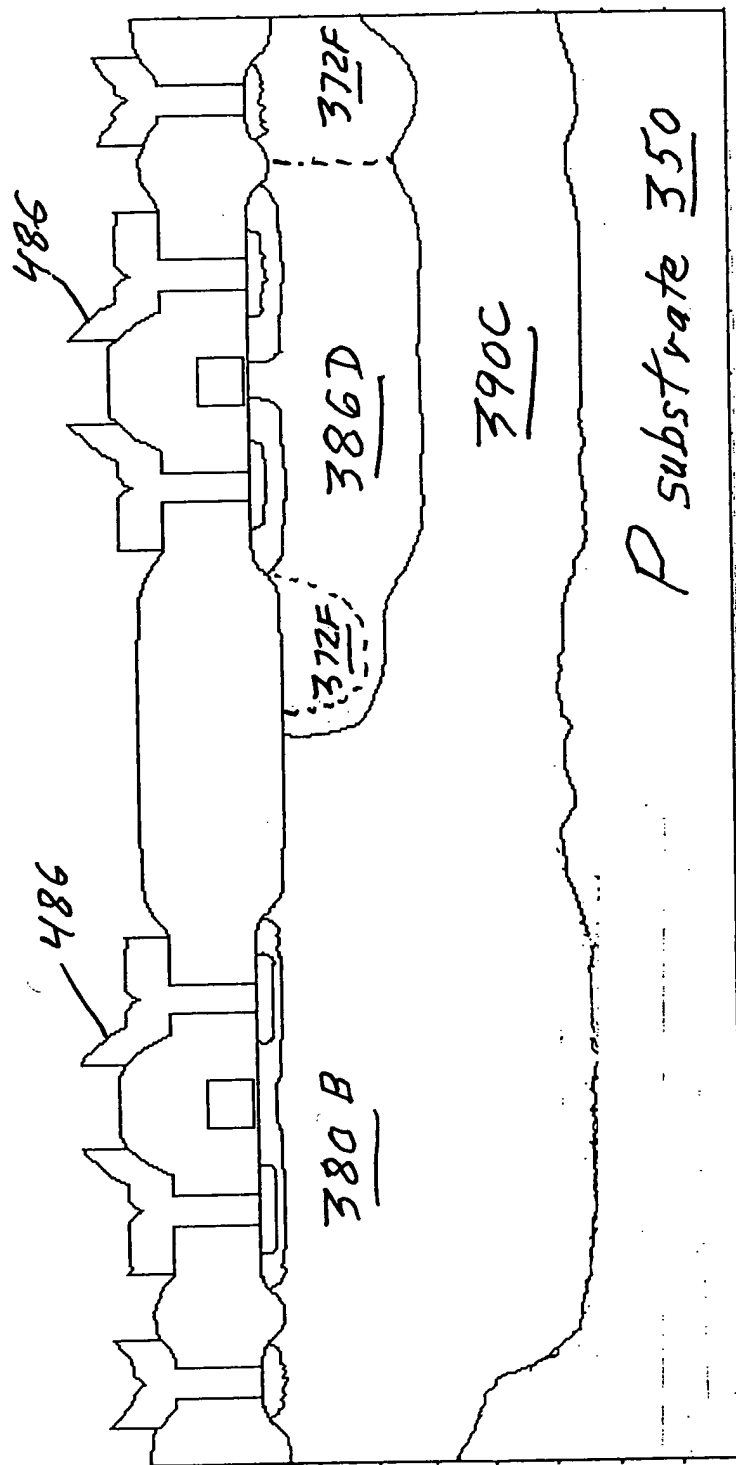
Metal layer  
Fig. 67C

30V Lateral Trench DMOS 308



Metal Layer  
Fig. 67D

Symmetrical 12V CMOS  
 12V PMOS 309 12V NMOS 310



Metal Layer  
 Fig. 67E

Fig. 17V

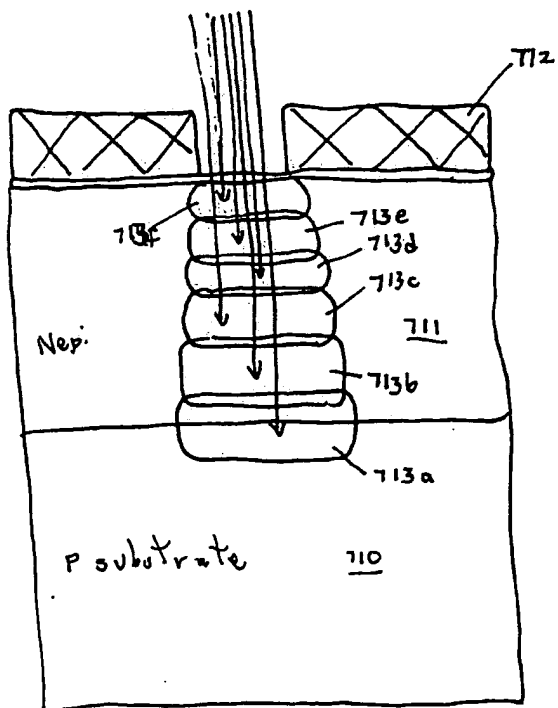


Fig. 17W

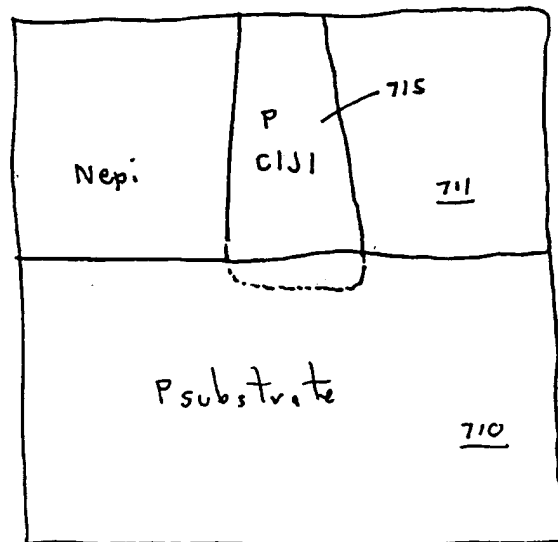


Fig. 17X

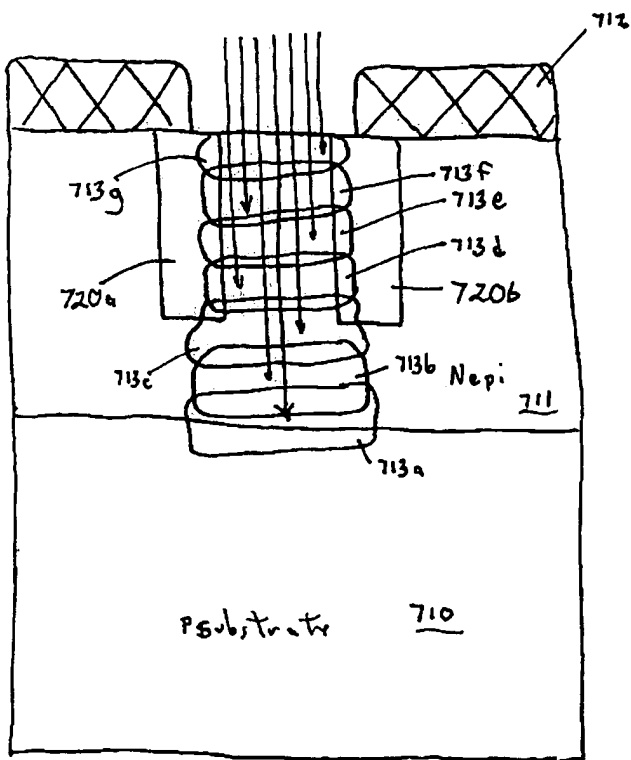


Fig. 17Y

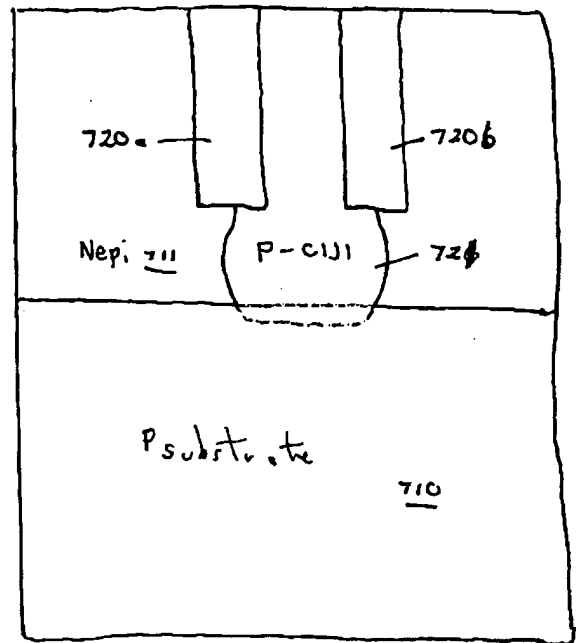




Fig. 17Z

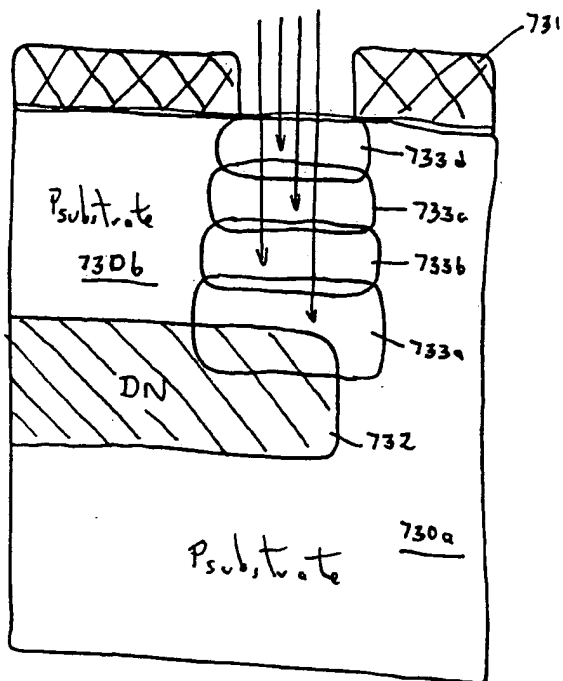


Fig. 17AA

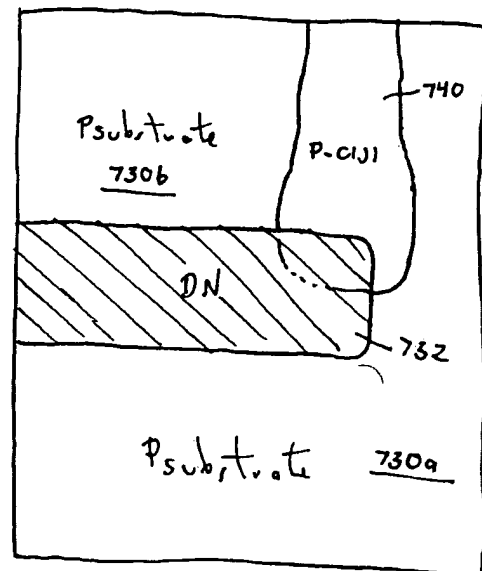


Fig. 17BB

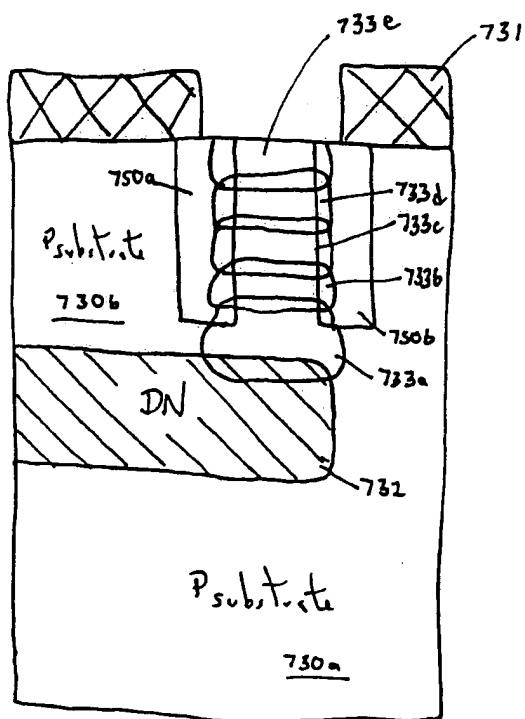


Fig. 17CC

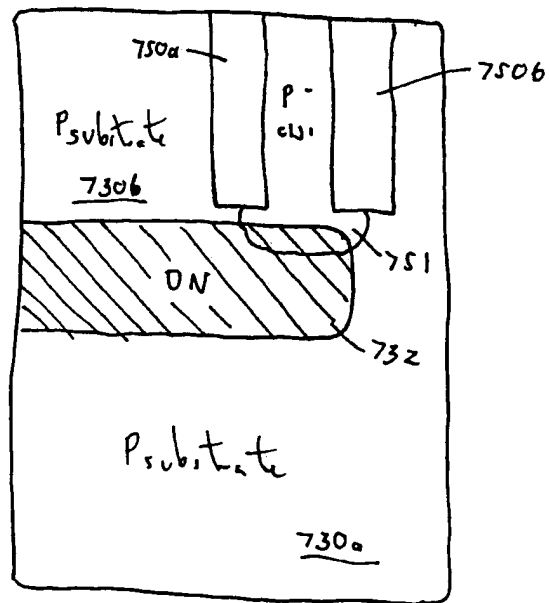


Fig. 18H

